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ATX
Ver: 1.1

Intel -Coffeelake plamform Z370

CPU:

Coffeelake-S

System Chipset:

Z370

Onboard Chip:

HD Audio Codec : ALC887

LAN : Intel I219

SIO : Nuvoton 6795

Flash ROM : 16MB GSE Z370

Main Memory:

DDRIV (800/1066/1333/1600/2133MHz) * 4 (Dual Channel)

ACPI:

NIKO/UPi

PWM:

UP9508

Expansion Slots:

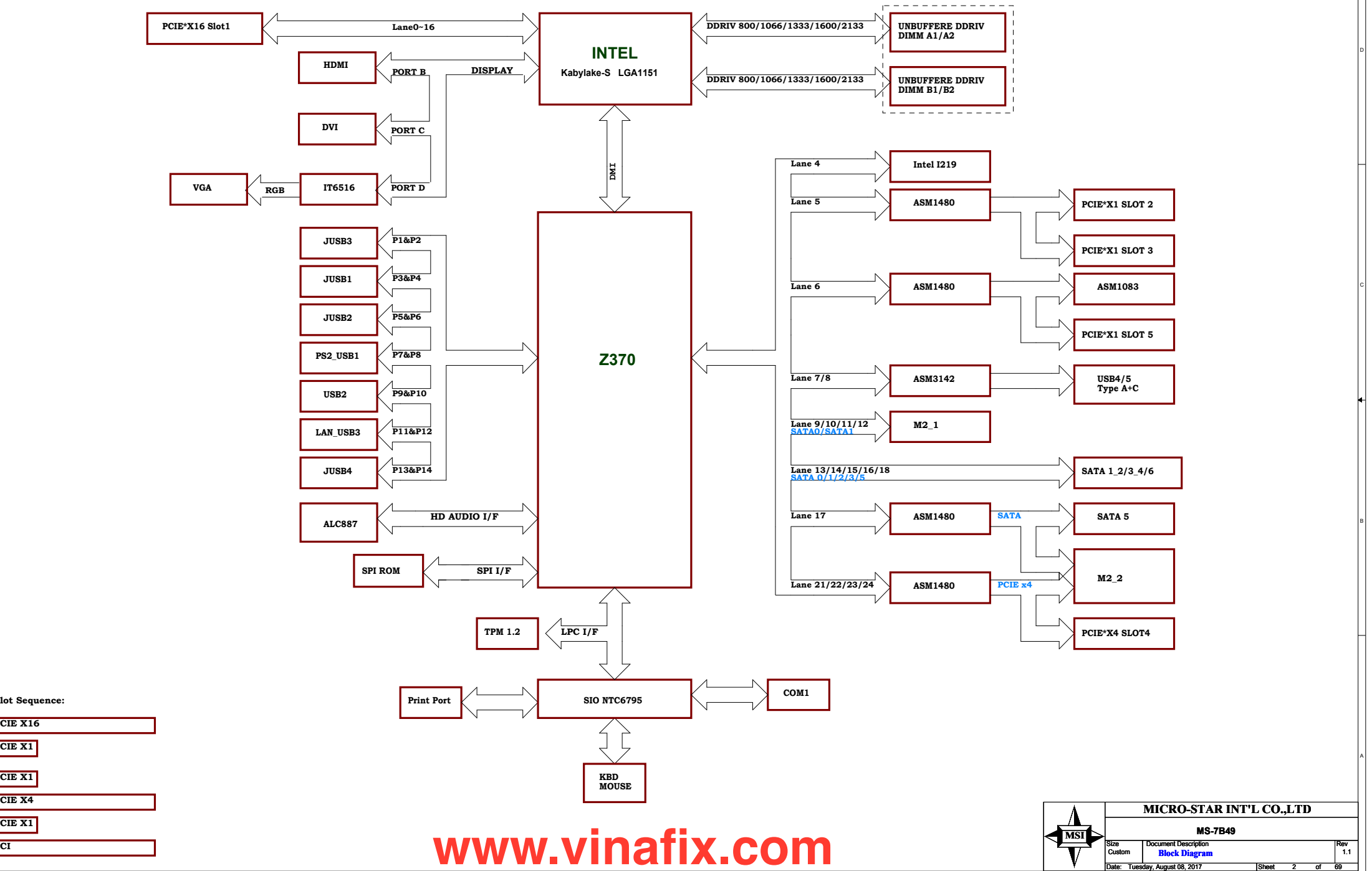
PCI Express (X16) Slot *1
PCI Express (X4) Slot * 1
PCI Express (X1) Slot * 3
PCI Slot * 1
M2 * 2 (22110 and 2280)

Other:

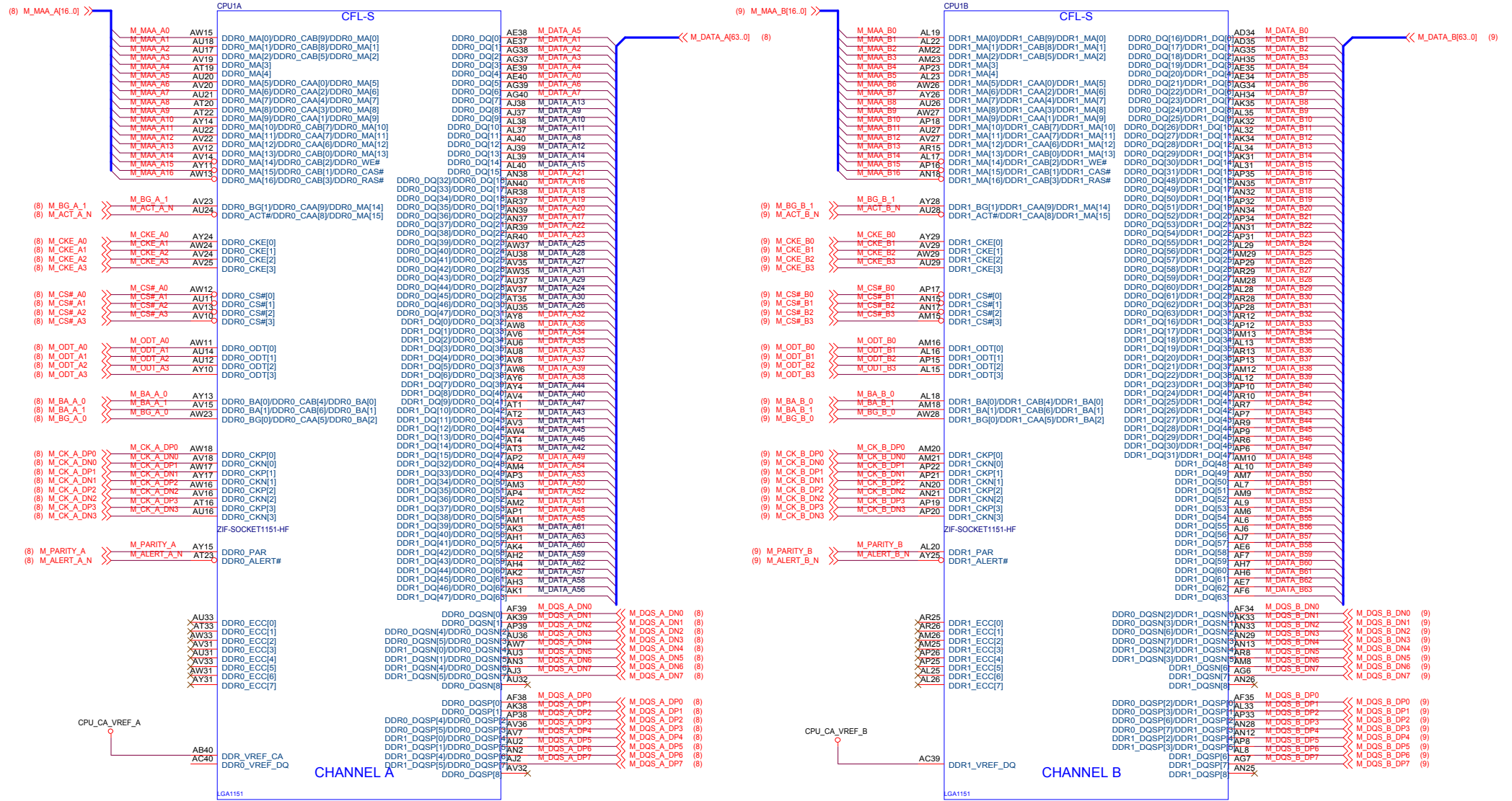
SATA3.0 x6 (PCH)
FRONT USB2.0 *4
FRONT USB3.0 *4
REAR USB2.0 *2
REAR USB3.0 *4
REAR USB3.1 TYPE A+C

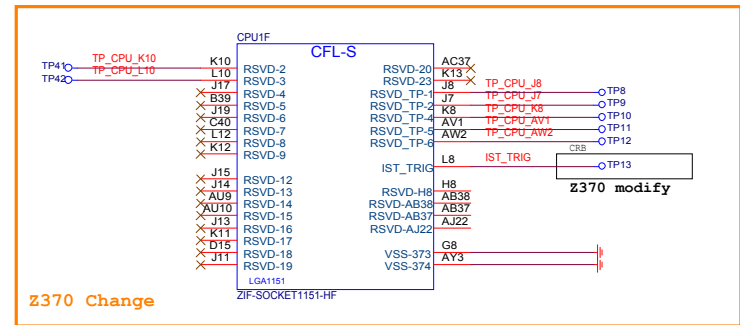
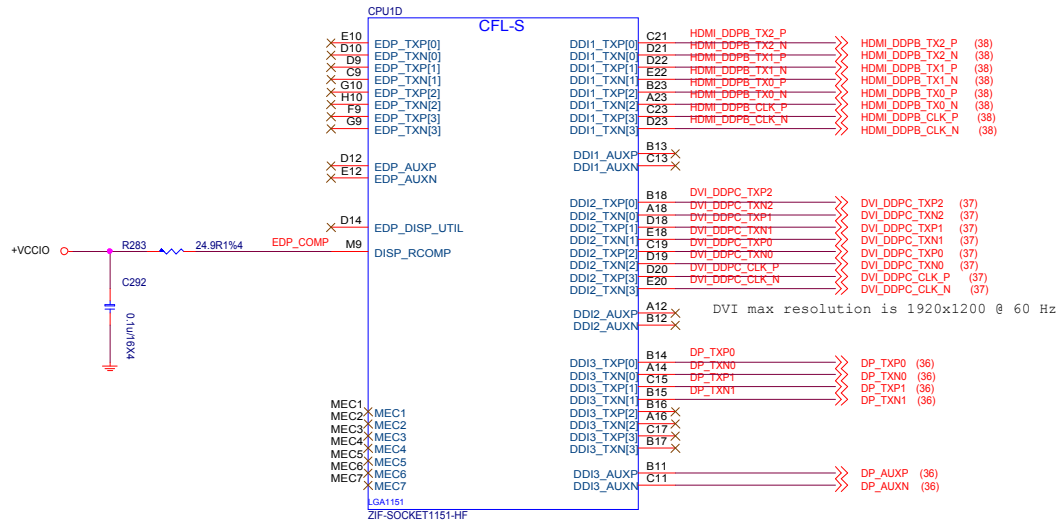
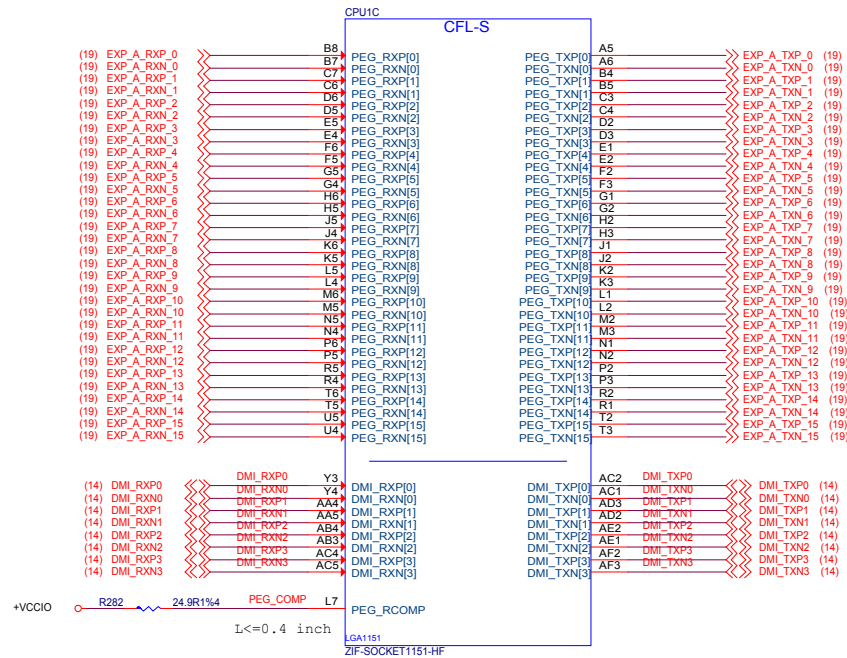
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MS-7B49 Block Diagram

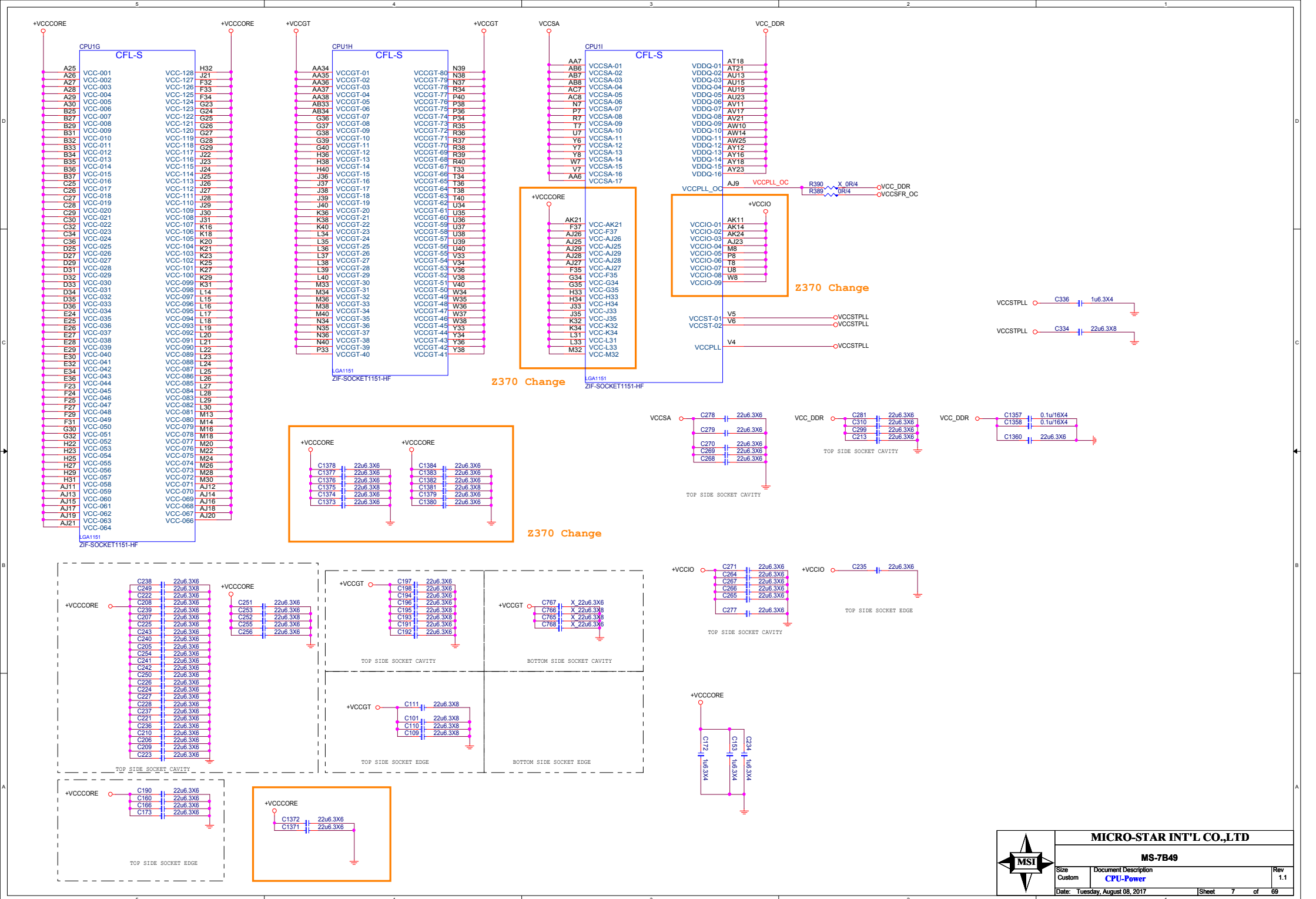


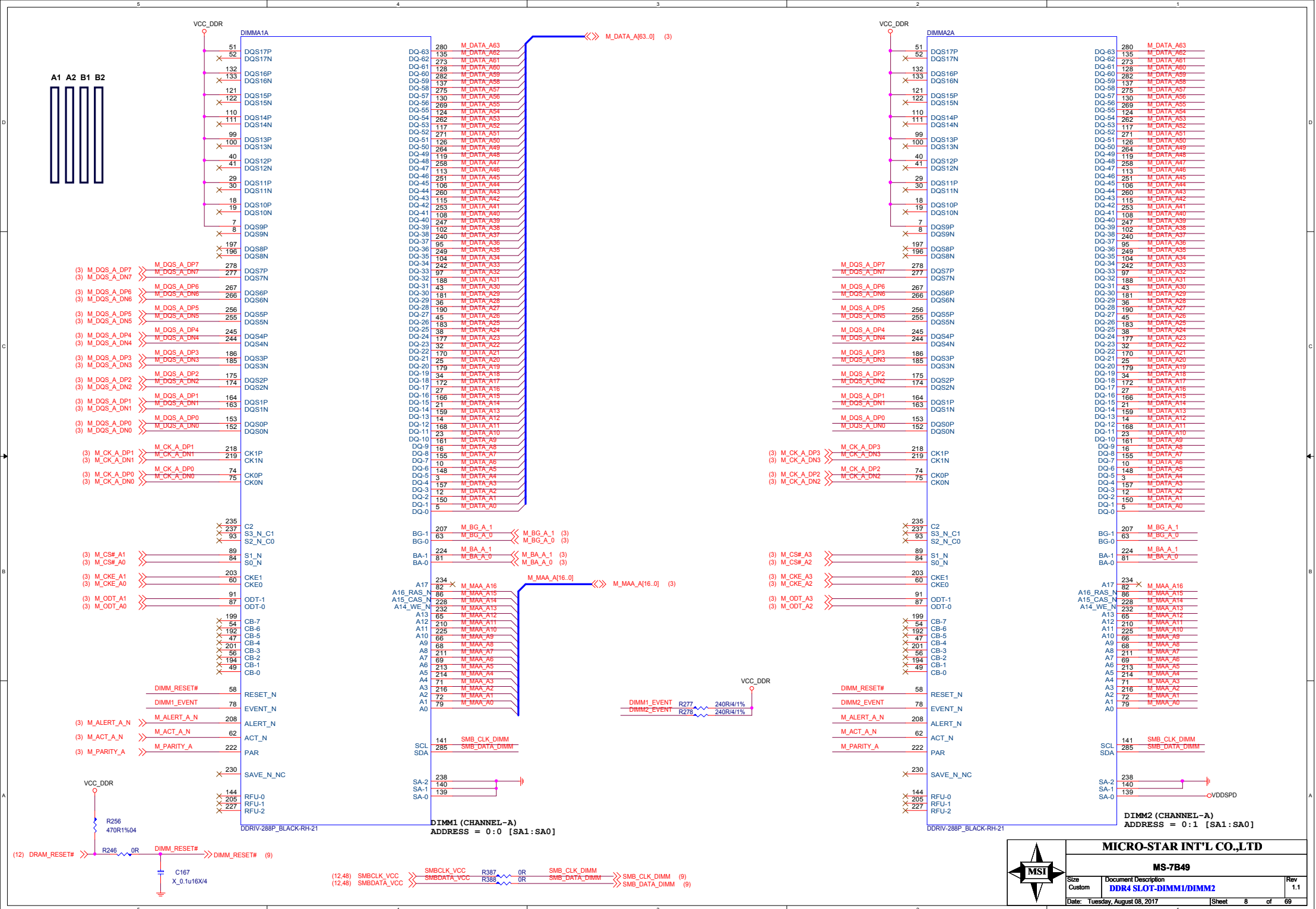
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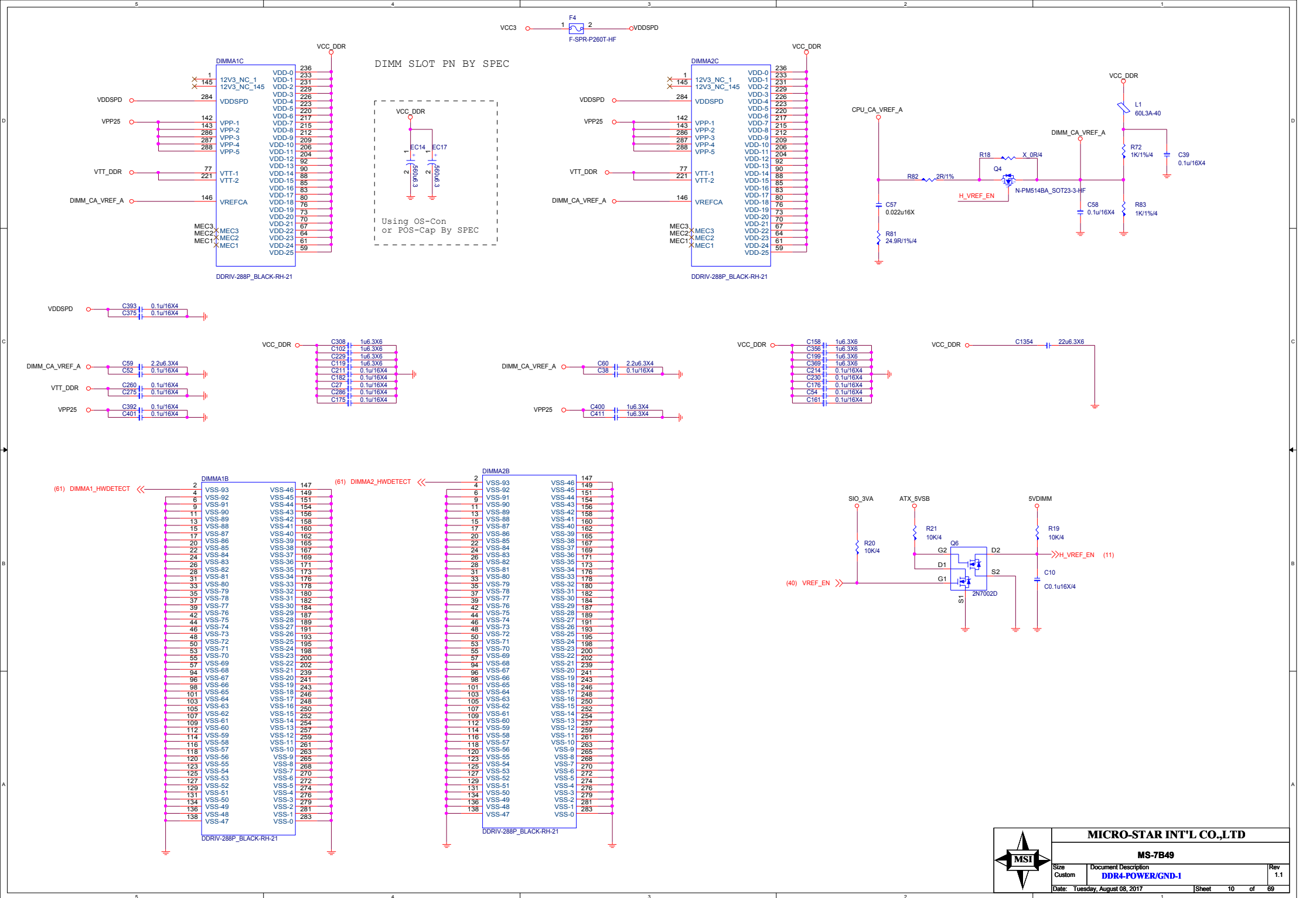


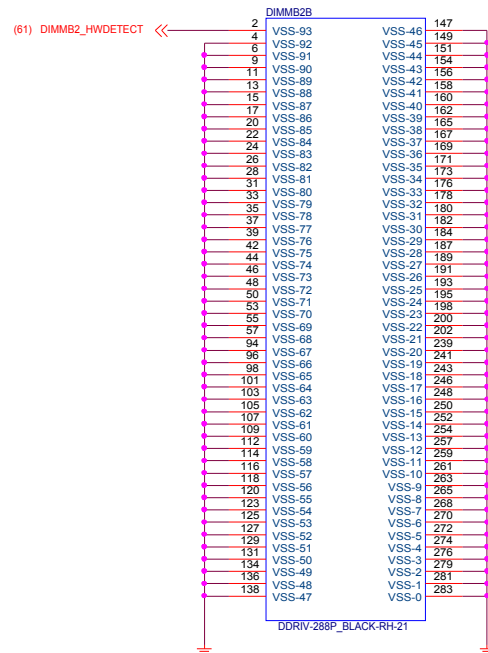
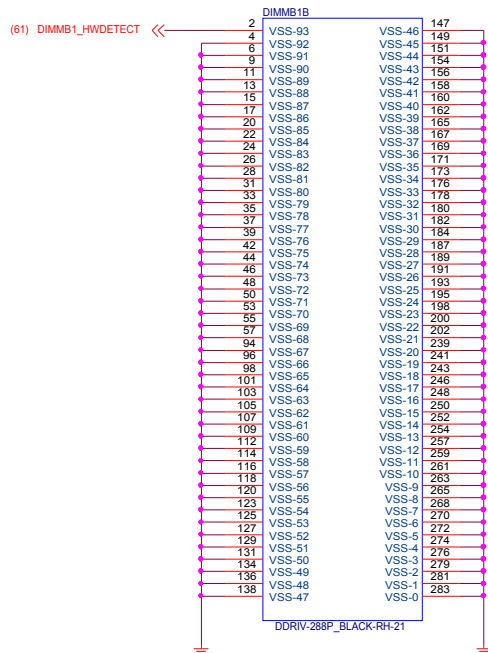
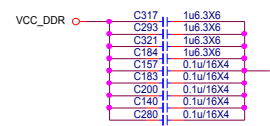
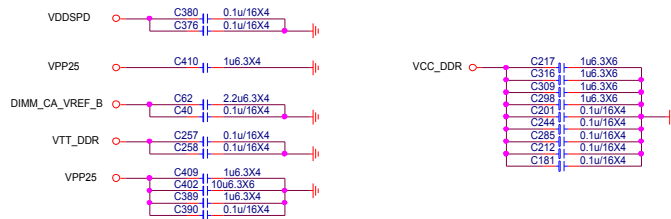
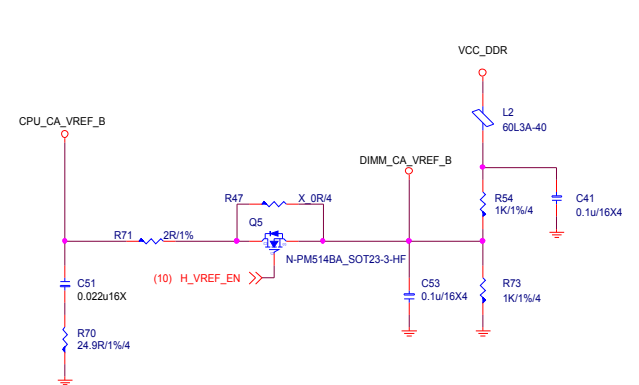
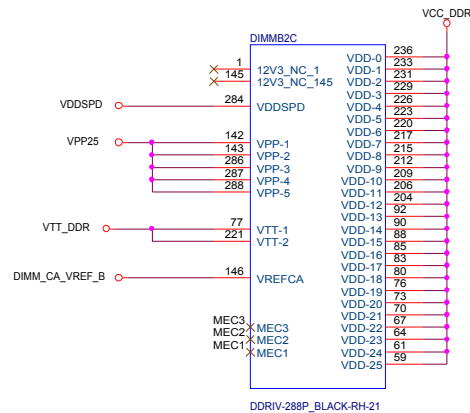
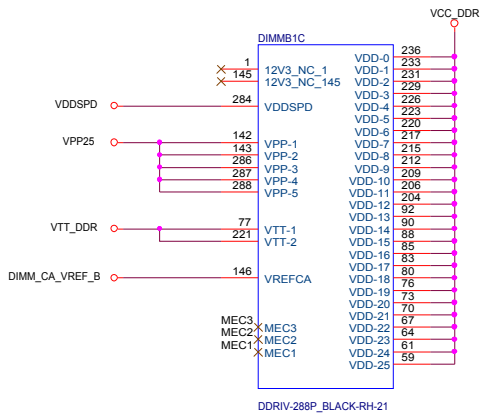


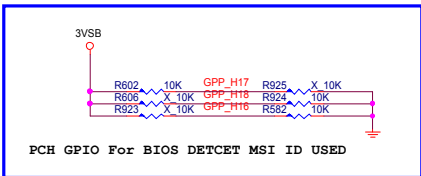
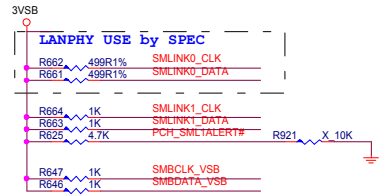
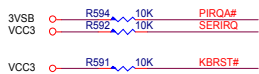
TP8, TP9, TP10, TP11, TP12, TP13, TP41, TP42
Reservd for CPU XDP debug pin



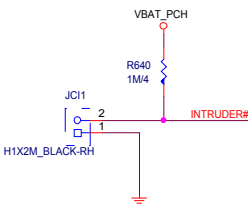




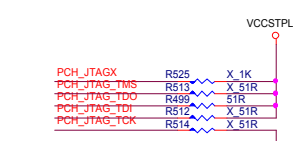
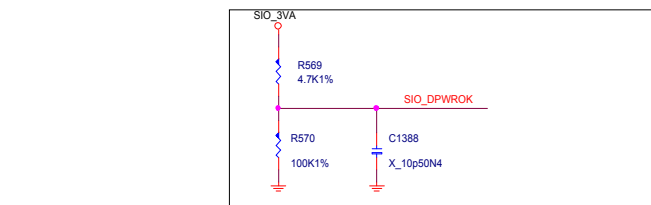
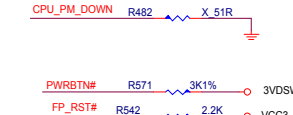
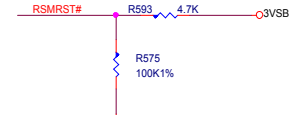
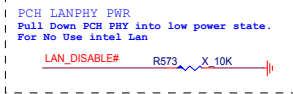
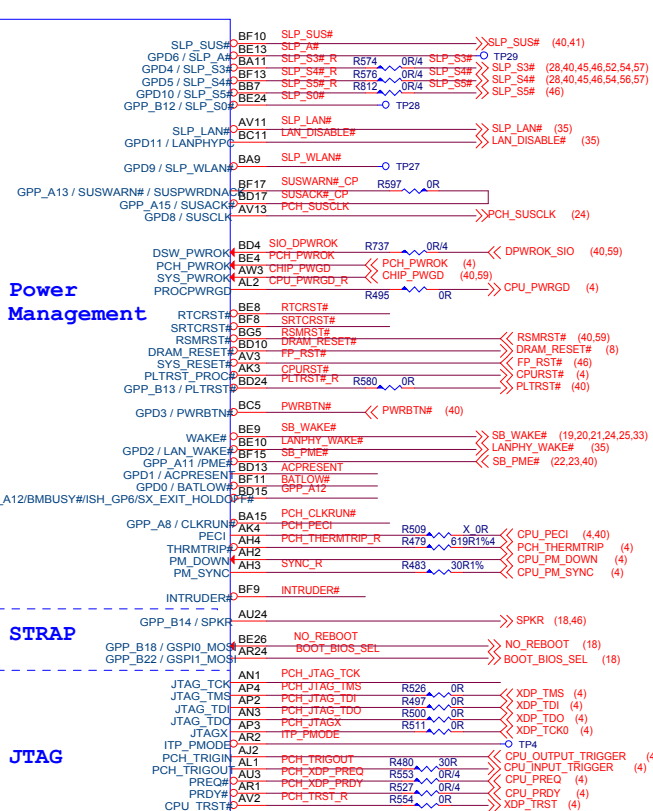
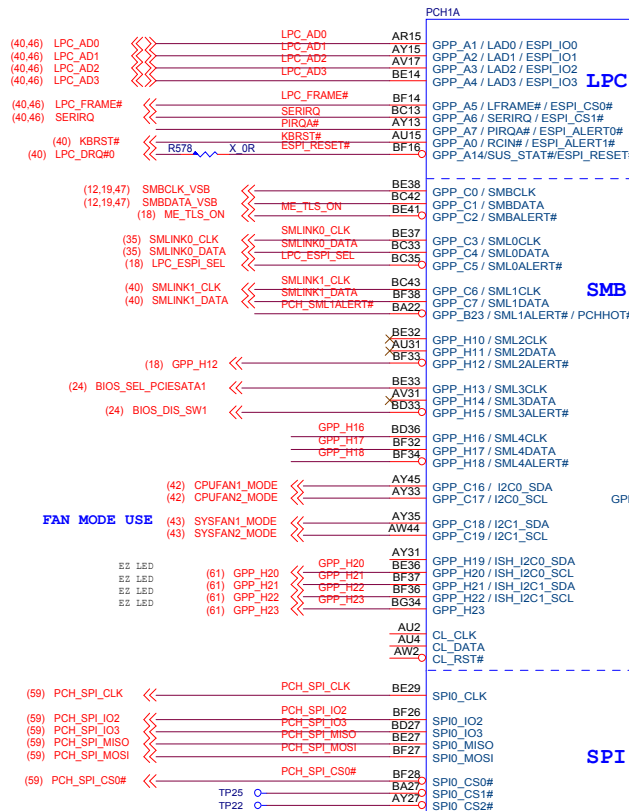
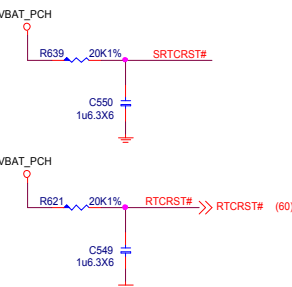




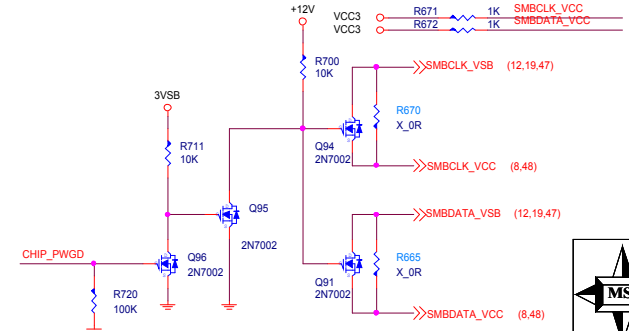
Chassis Intrusion



RTC



擺在一起 (注意到所有的SMBUS的分枝)

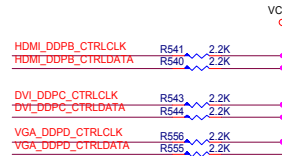
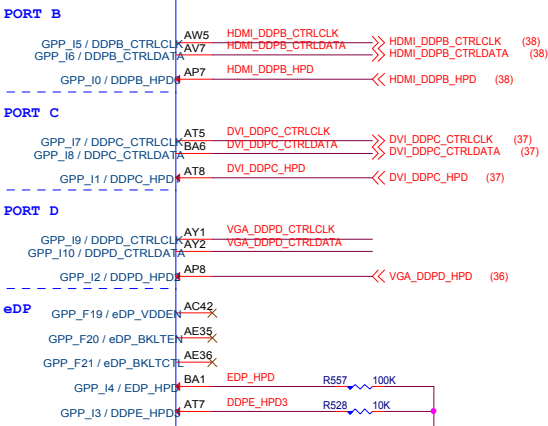
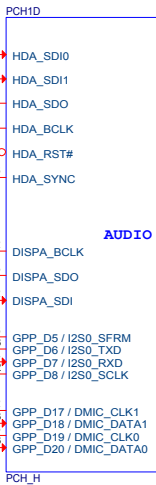
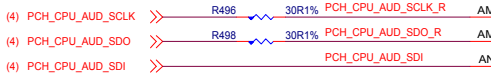
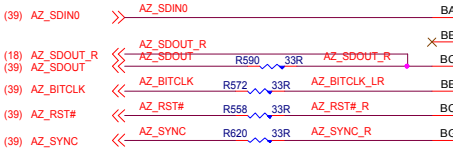
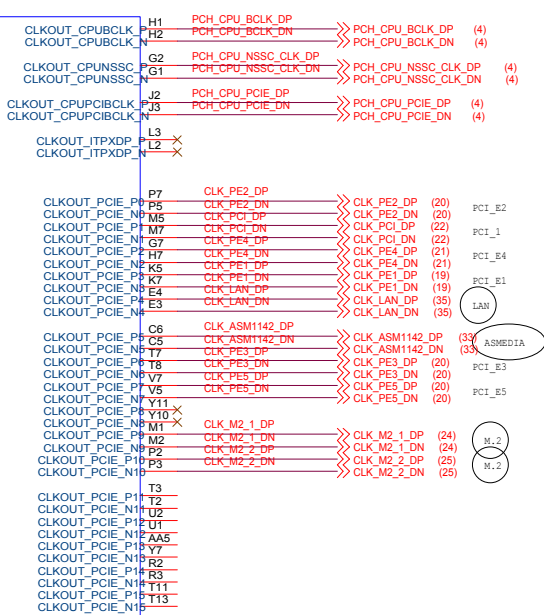
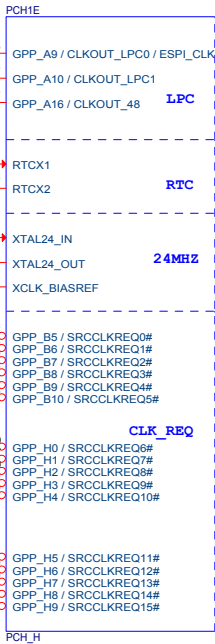
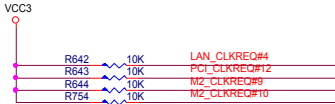
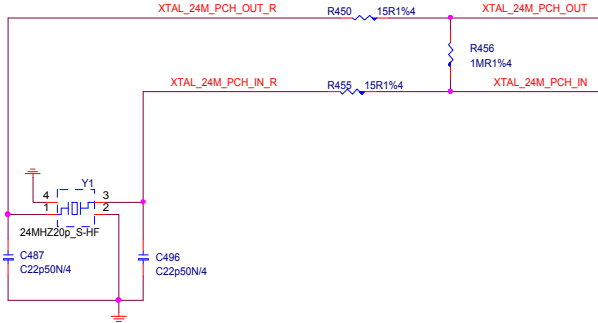
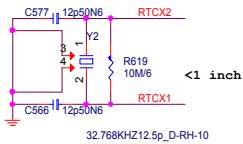


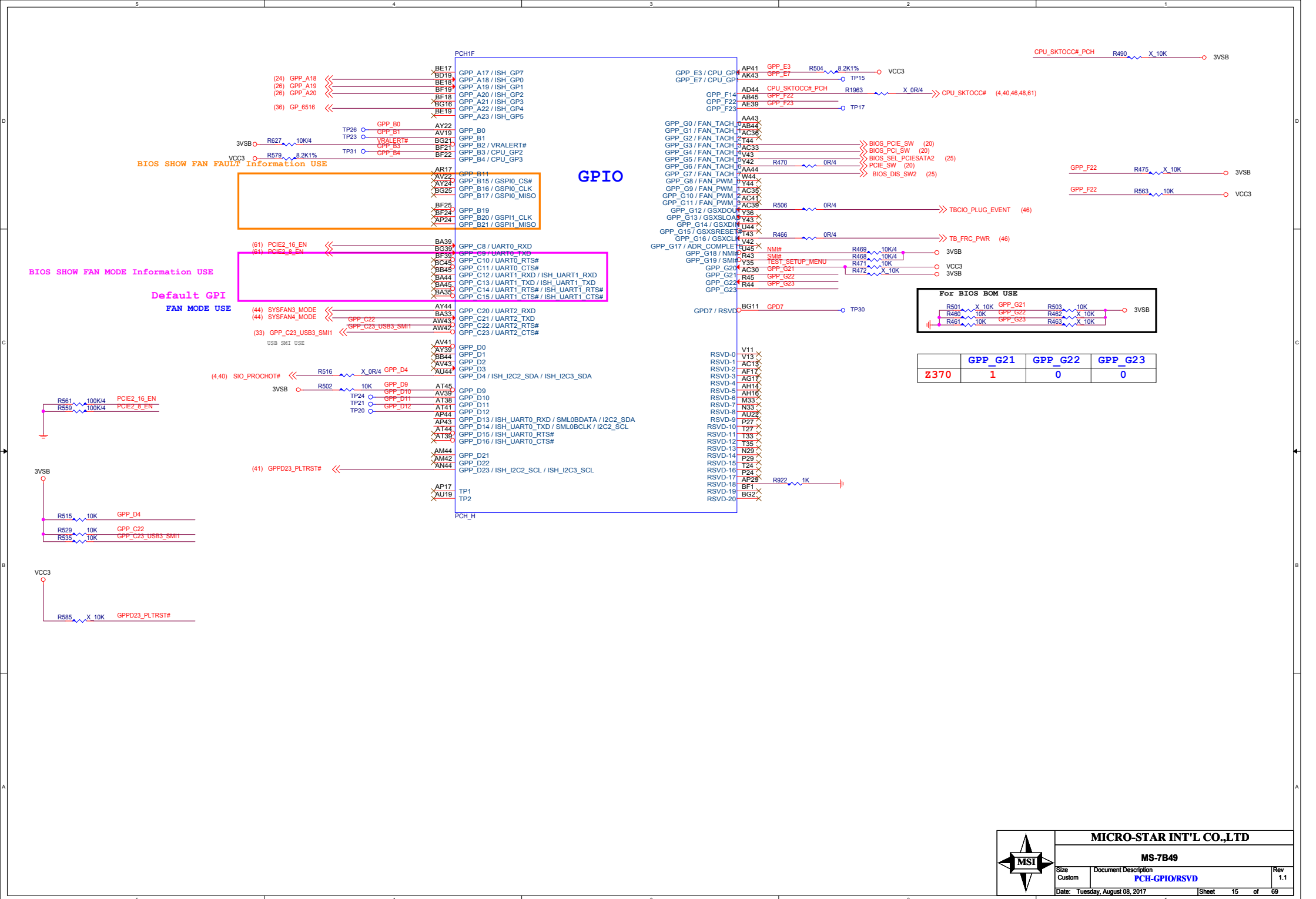
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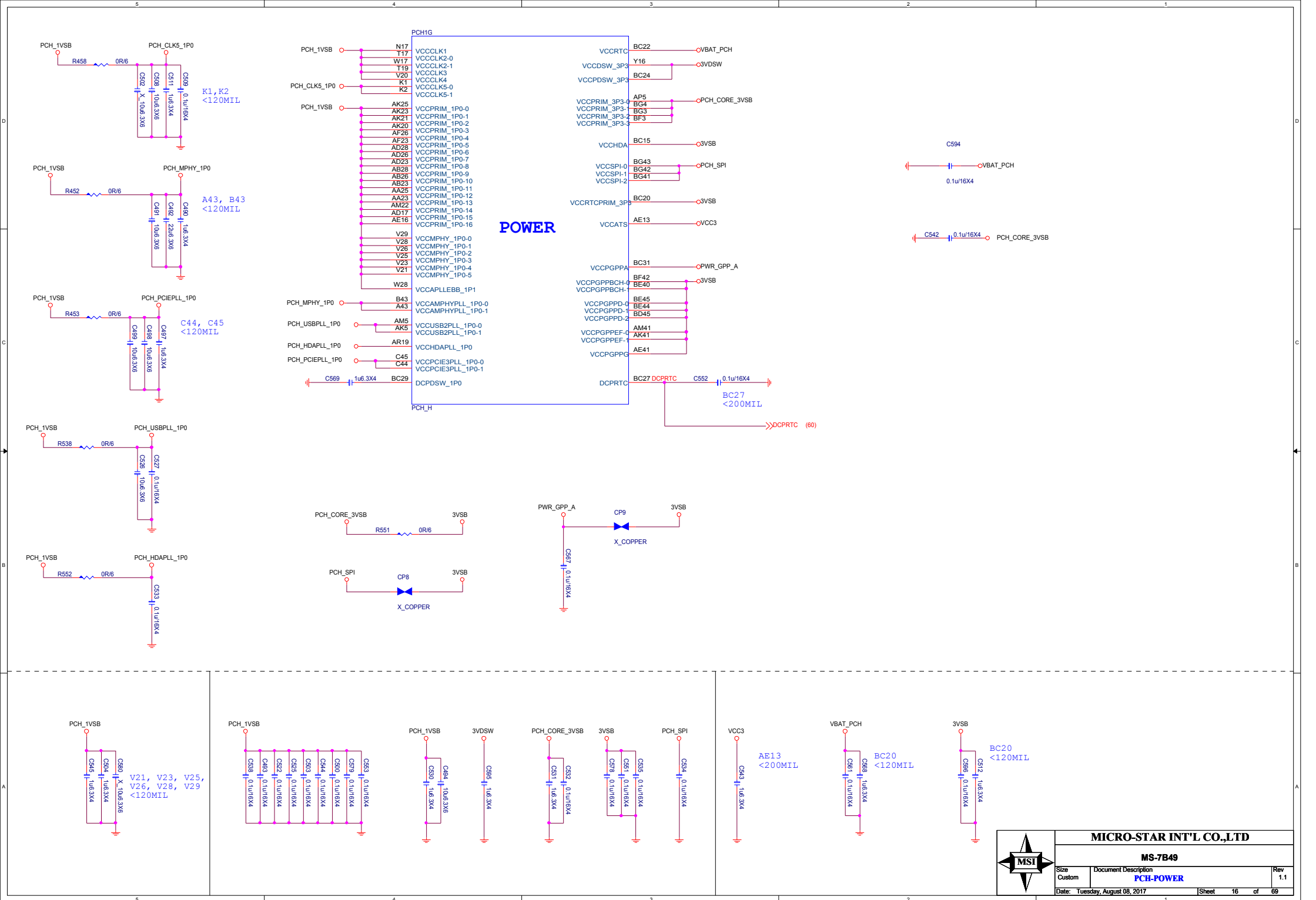
PCH_CLK

RTC Block

Close to PCH

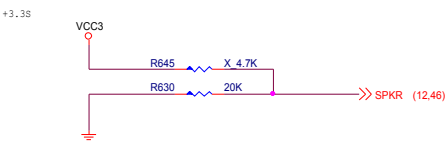






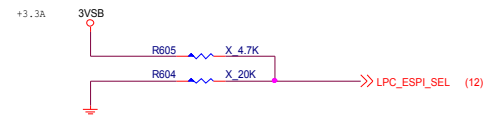
VSS

TOP Swap



Internal pull-down is disabled after PLTRST#

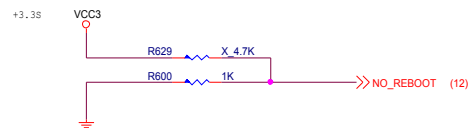
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down is disabled after RSMRST

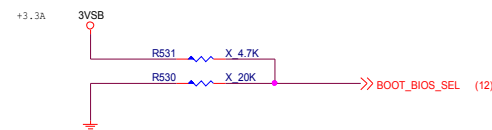
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down is disabled after PLTRST#

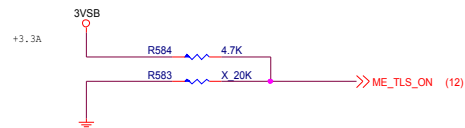
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down is disabled after PLTRST

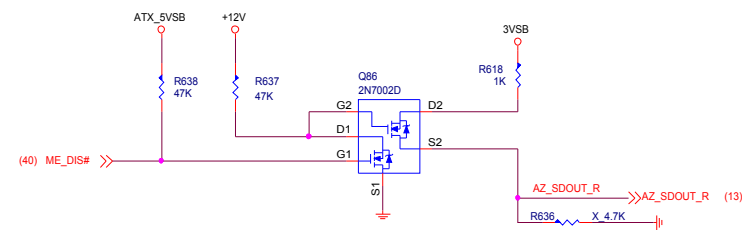
AMT and SBA with confidentiality



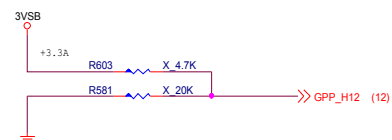
0 : DISABLE
1 : ENABLE (Default)

Internal pull-down is disabled after RSMRST

HDA_SDO



ESPI FLASH SHARING MODE

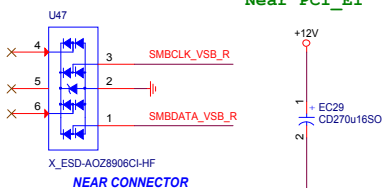
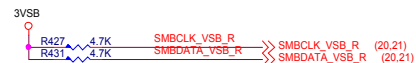


0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

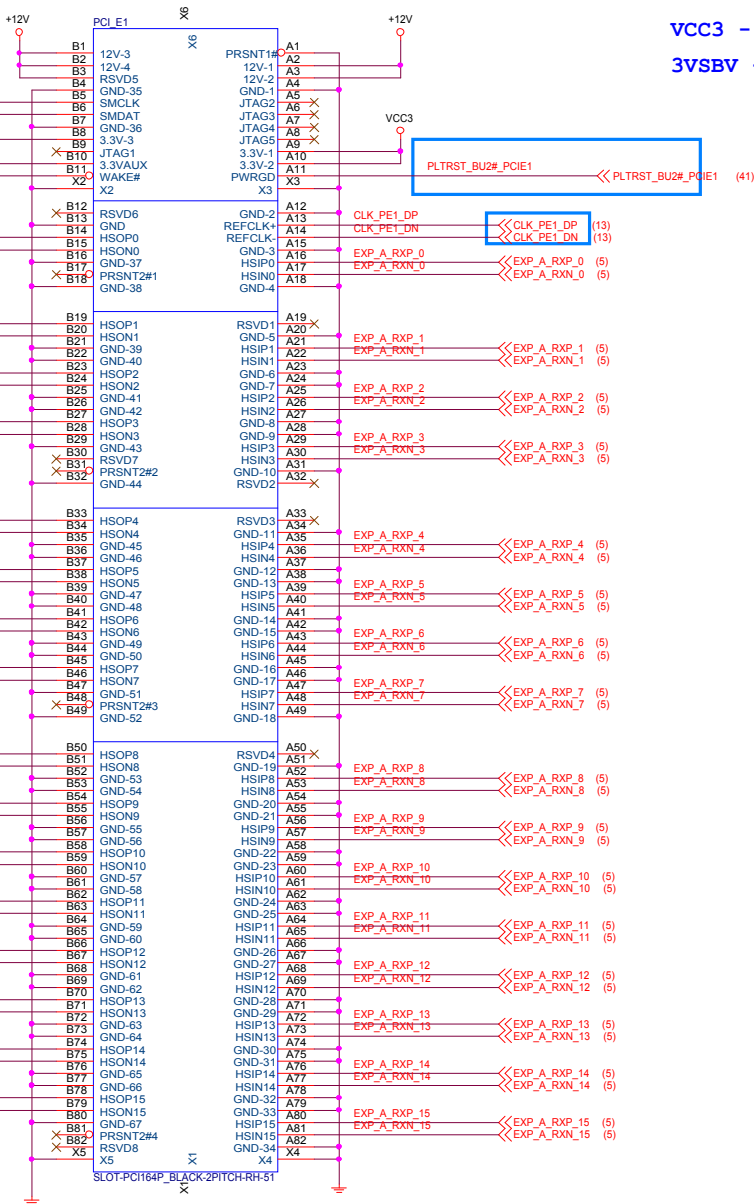
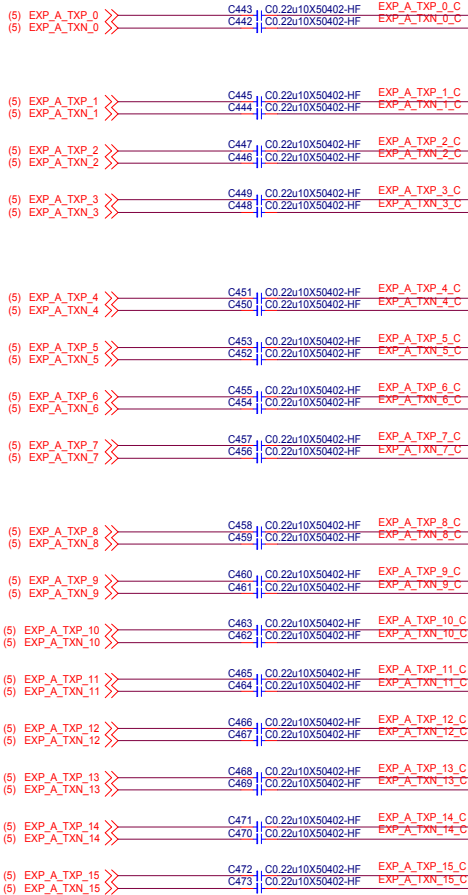
Internal pull-down is disabled after RSMRST

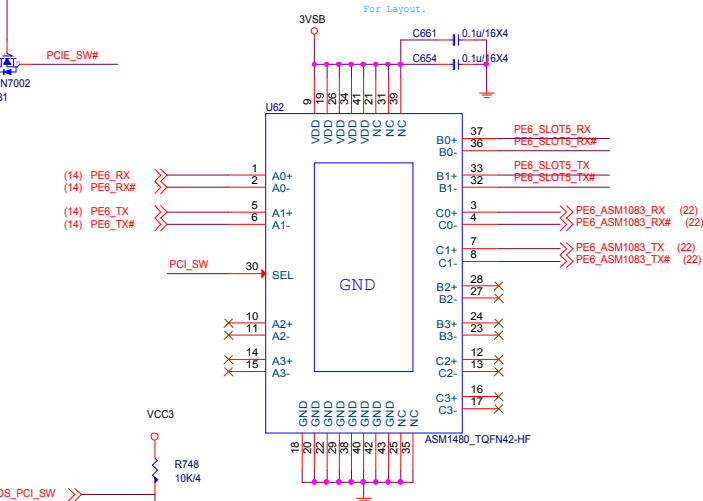
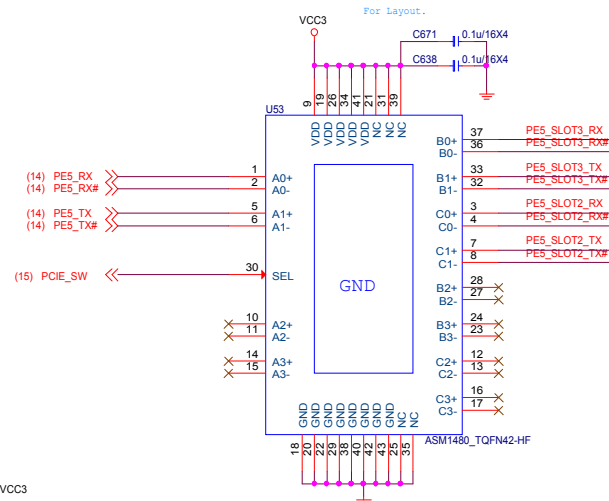
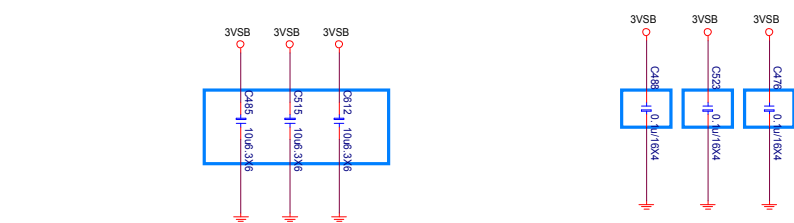
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12V - 5.5A
VCC3 - 3A
3VSB - 375mA



(12,20,21,24,25,33) SB_WAKE# <<

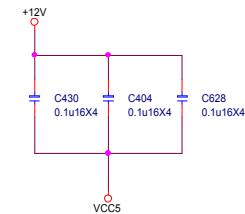
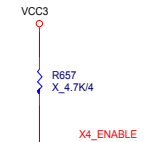




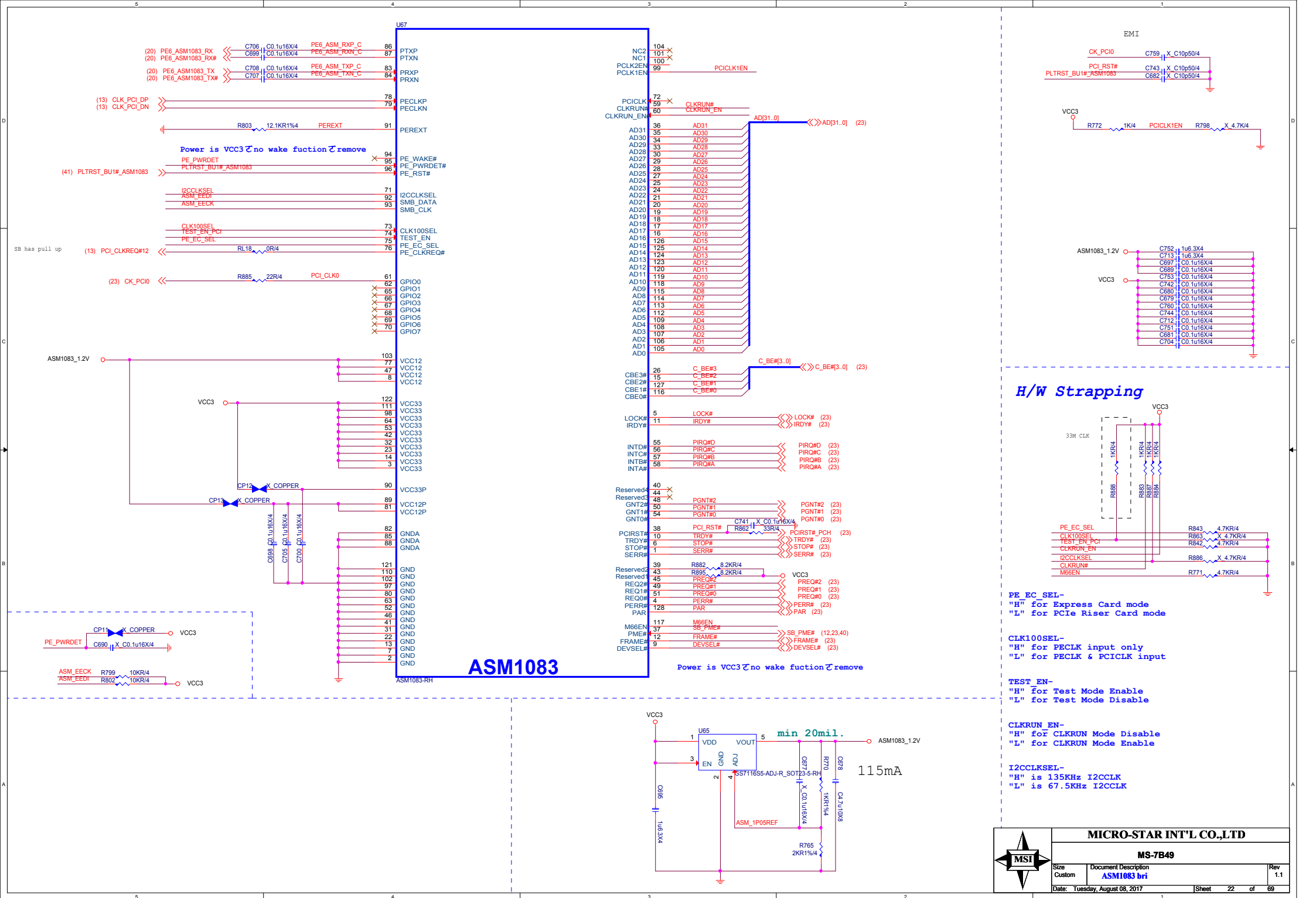
MS-7B49

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12V - 2.1A
VCC3 - 3A
3VSBV - 375mA



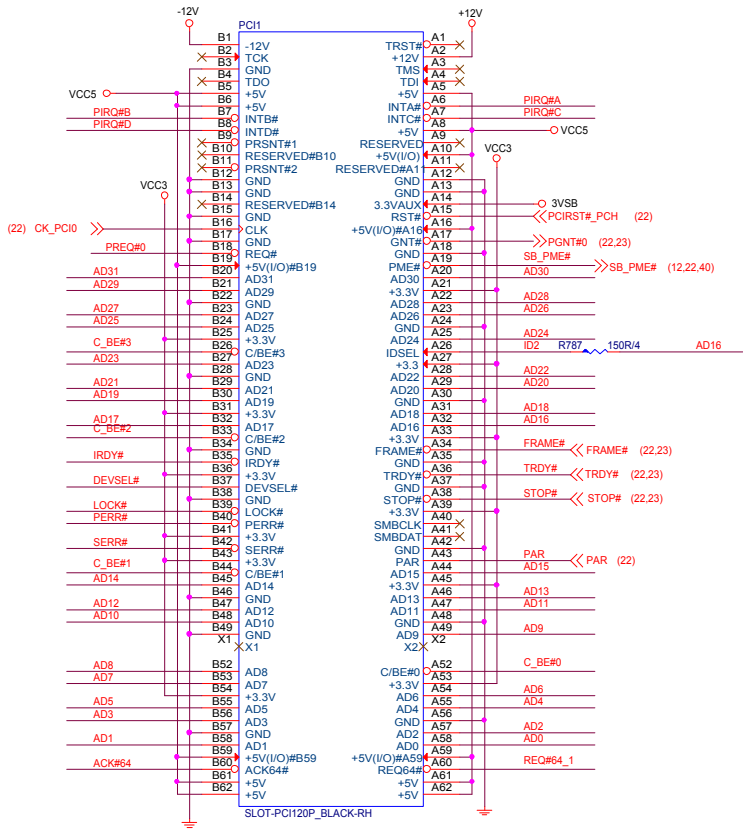
Size Custom	Document Description PCIE SLOT (X4)	Rev 1.1
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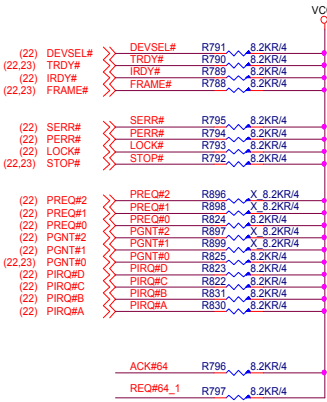
PCI

3.3Vaux:0.375*2=0.75A (wake)
0.02*2=0.04A (no wake)
VCC3 :7.6*2=15.2A
VCC5:5*2=10A
+12V:0.5*2=1A
-12V:0.1*2=0.2A

AD[31..0] <<>> AD[31..0] (22)
C_BE#[3..0] <<>> C_BE#[3..0] (22)

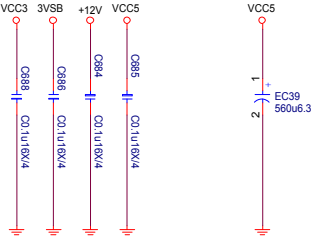


PCI PULL-UP / DOWN RESISTORS



IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

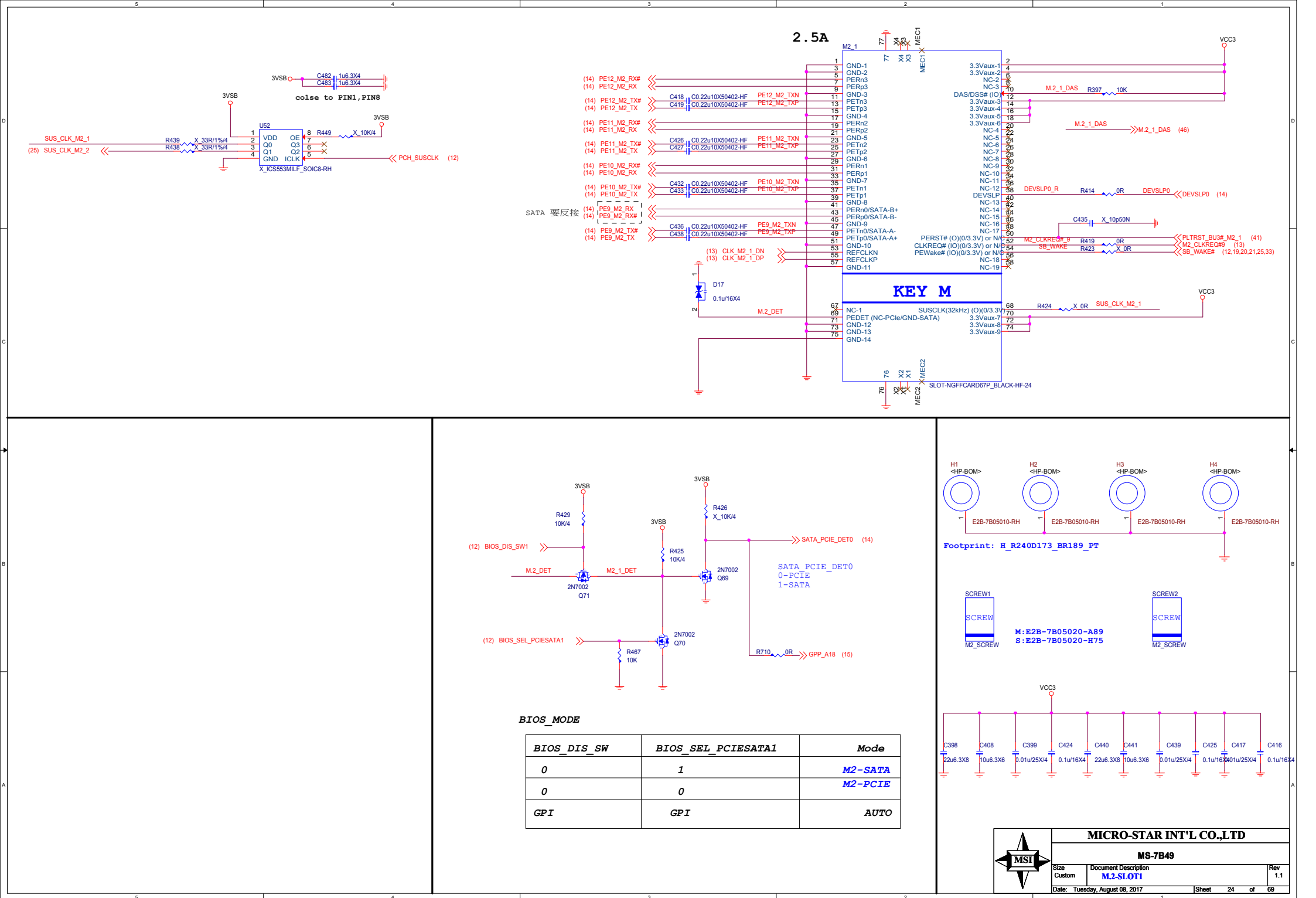
EMI:close pin

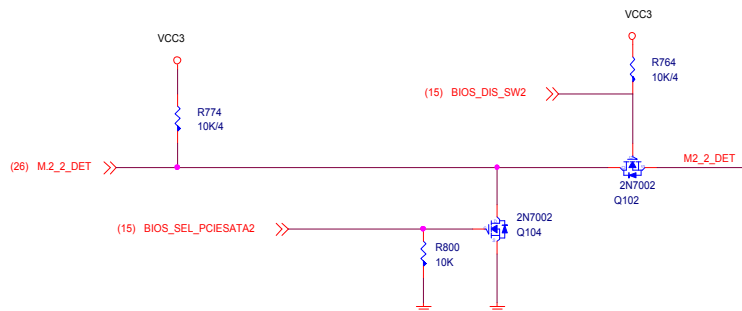
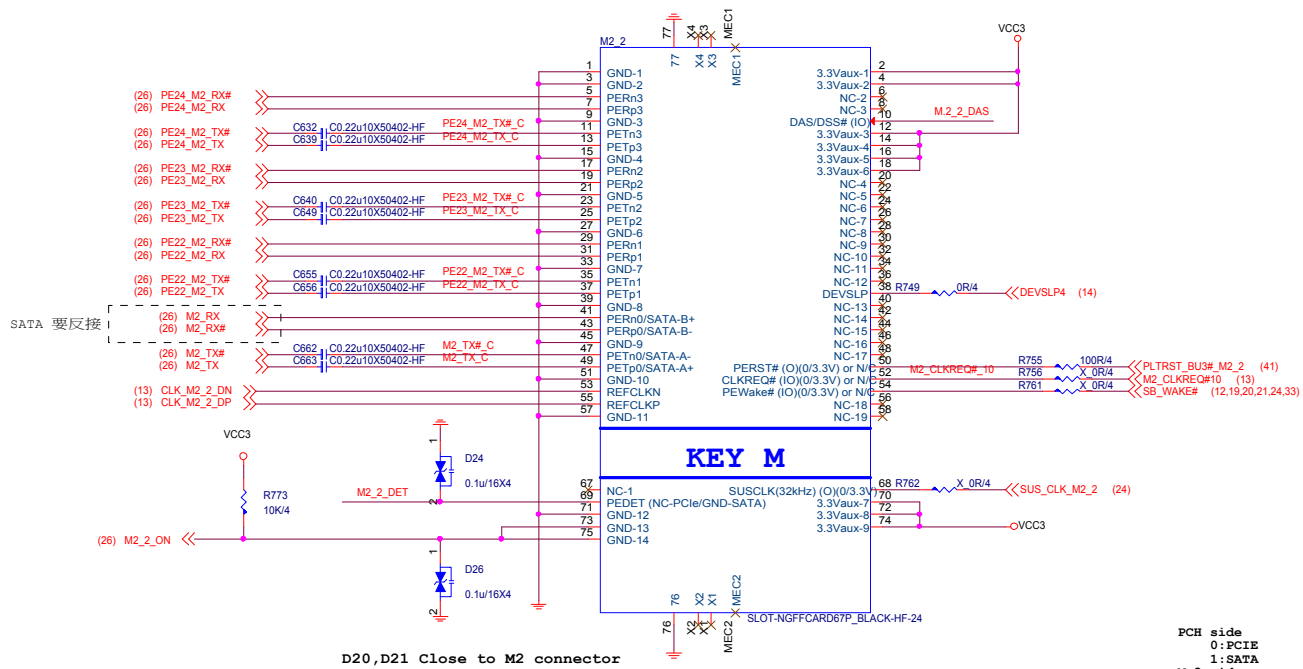


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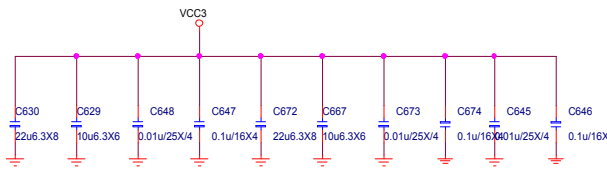
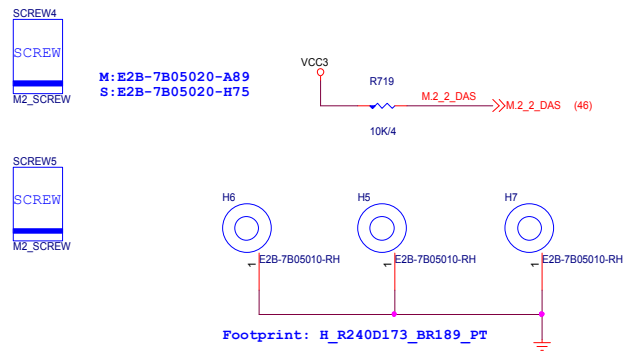
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BIOS_MODE

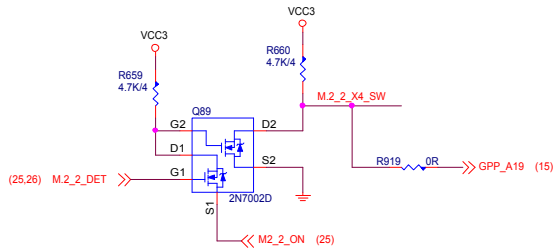
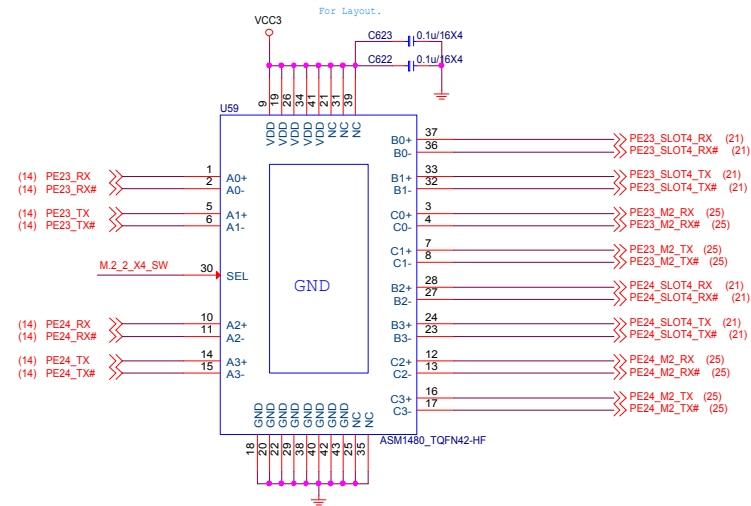
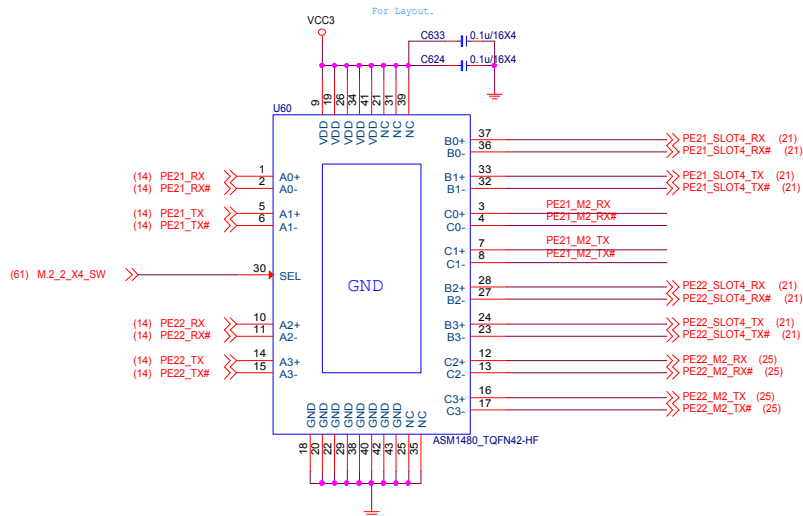
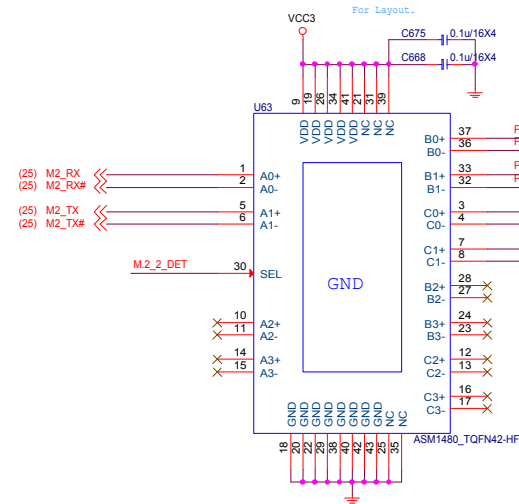
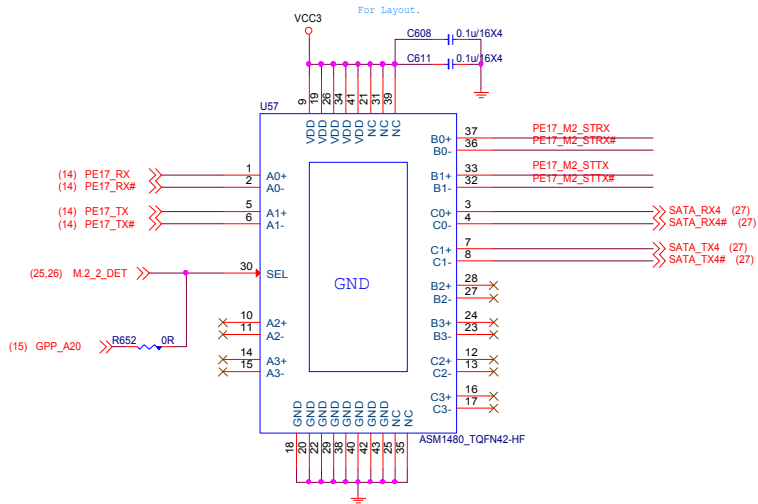
BIOS_DIS_SW2	BIOS_SEL_PCIESATA2	Mode
1	0	M2-PCIE
0	1	X4 SLOL-PCIE
GPI	GPI	GPI



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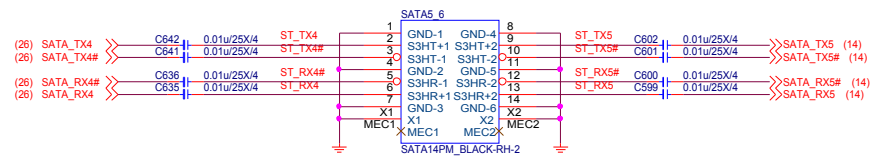
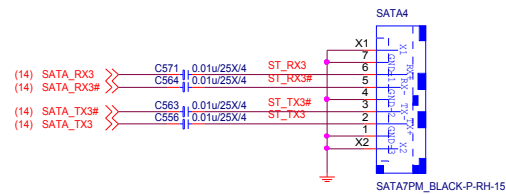
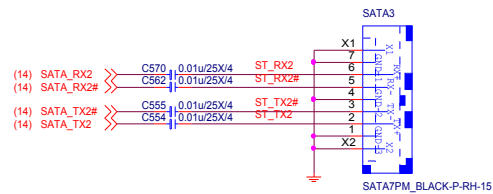
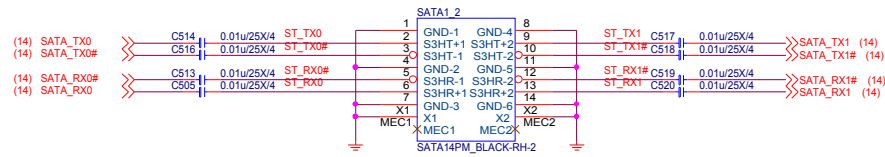


Default
M.2_2 PCIE
M.2_2 SATA

M.2_2_ON	M.2_2_X4_SW	M.2 SATA	M.2 PCIE	X4 SLOT	SATA5
V	V	X	X	V	V
X	X	X	V	X	V
X	V	V	X	V	X



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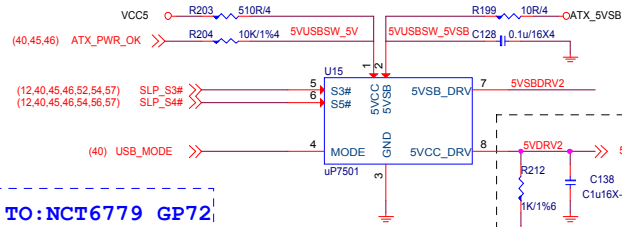


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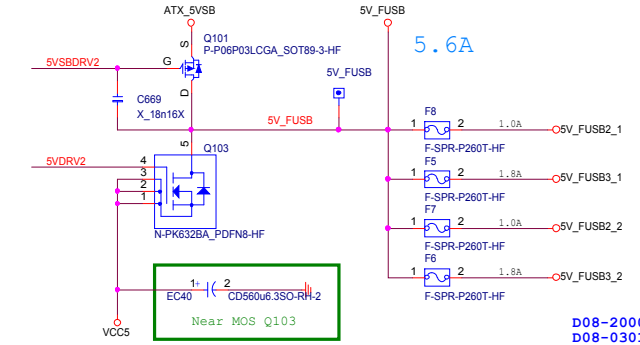
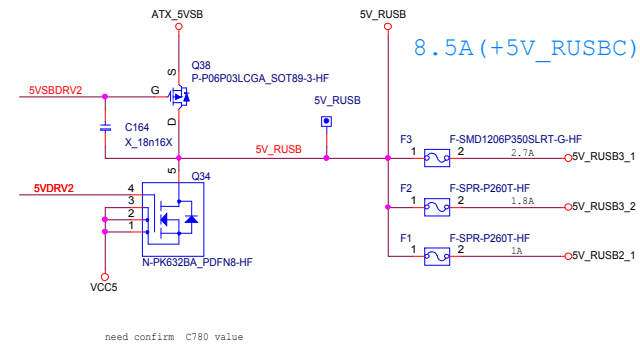
MS-7B49

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REAR USB PORT POWER



5VDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.



P-MOS
D03-06P0319-N03

N-MOS
D03-510BA0C-N03
D03-3056M00-U47
D03-4C05N03-O05
D03-3830D09-N47
D03-632BA0C-N03

D08-2000400-P16 (Itrip=3.5A; 0.003ohm)
D08-0301000-P16 (Itrip=2.6A; 0.015ohm)

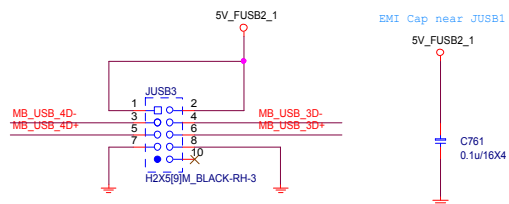
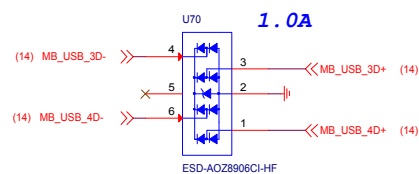
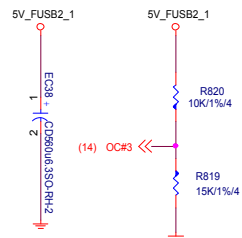


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Diagram illustrating the structure of RN13 and RN14. RN13 is a 40-nucleotide RNA with a 2:2:2:2 tetraloop structure. It has MB_USB_3D+ at the 5' end and MB_USB_3D- at the 3' end. RN14 is a 40-nucleotide RNA with a 2:2:2:2 tetraloop structure. It has MB_USB_4D+ at the 5' end and MB_USB_4D- at the 3' end. Both RNAs are shown with their sequences and the positions of the loops.



The image shows two schematic diagrams of 4P2R-0R0402 components, labeled RN12 and RN11.

Diagram 1 (RN12): This component has four pins. Pin 1 is connected to MB_USB_5D+, Pin 2 to MB_USB_5D-, Pin 3 to MB_USB_5D-, and Pin 4 to MB_USB_5D+.

Diagram 2 (RN11): This component has four pins. Pin 1 is connected to MB_USB_6D+, Pin 2 to MB_USB_6D-, Pin 3 to MB_USB_6D-, and Pin 4 to MB_USB_6D+.

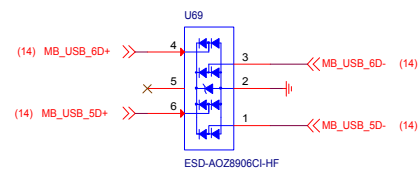
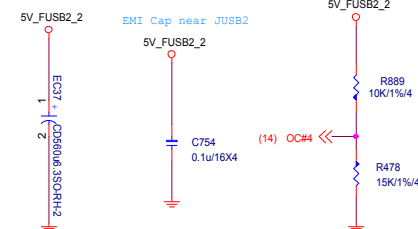


Figure 1-6A shows the USB2_2 connector pinout and signal traces. The top part is a connector pinout for JUSB4. The pins are numbered 1 through 10. The connections are as follows:

- Pins 1, 2, 3, and 4 are connected to MB_USB_5D-, MB_USB_5D+, MB_USB_6D-, and MB_USB_6D+ respectively.
- Pins 5, 6, 7, and 8 are connected to HZK5[9]M_BLACK-RH-3.
- Pins 9 and 10 are connected to ground.

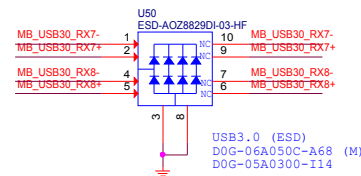
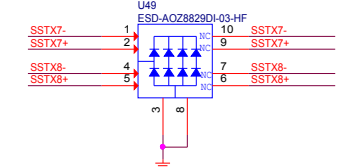
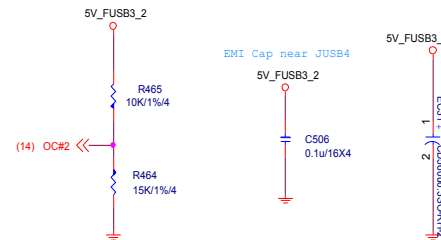
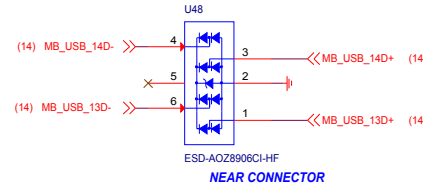
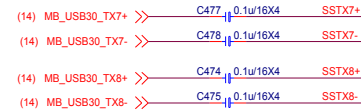
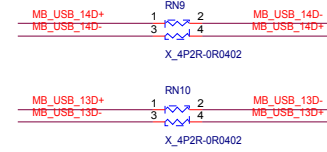
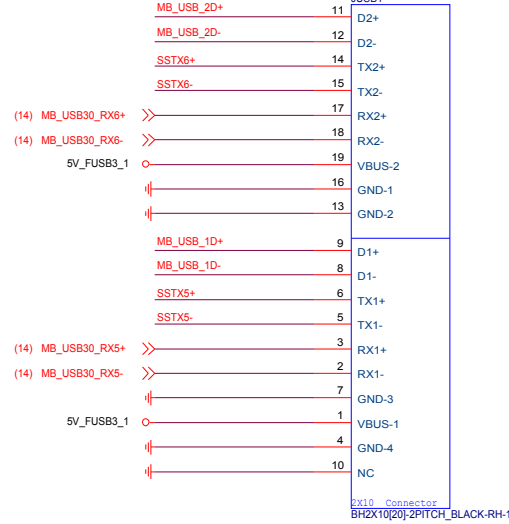
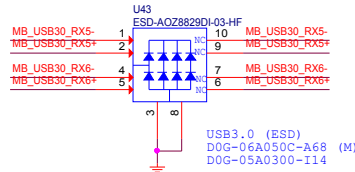
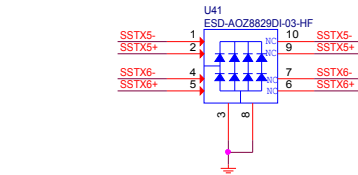
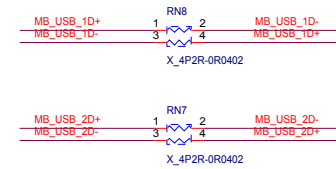
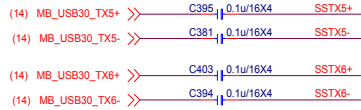
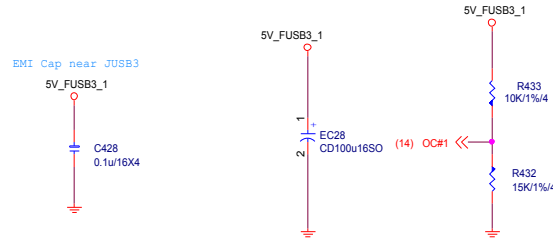
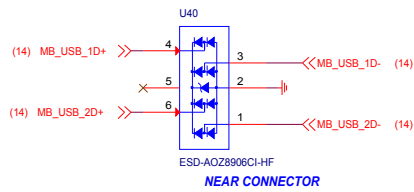
The bottom part shows three signal traces:

- 5V_FUSB2_2**: A trace connected to the 5V_FUSB2_2 pin of the connector.
- EMI37+**: A trace connected to the EMI37+ pin of the connector.
- 5V_FUSB2_2**: A trace connected to the 5V_FUSB2_2 pin of the connector, passing through a capacitor C754 (0.1u/16X4) to ground.
- 5V_FUSB2_2**: A trace connected to the 5V_FUSB2_2 pin of the connector, passing through a resistor R889 (10K/1%/4) and a resistor R478 (15K/1%/4) to ground.

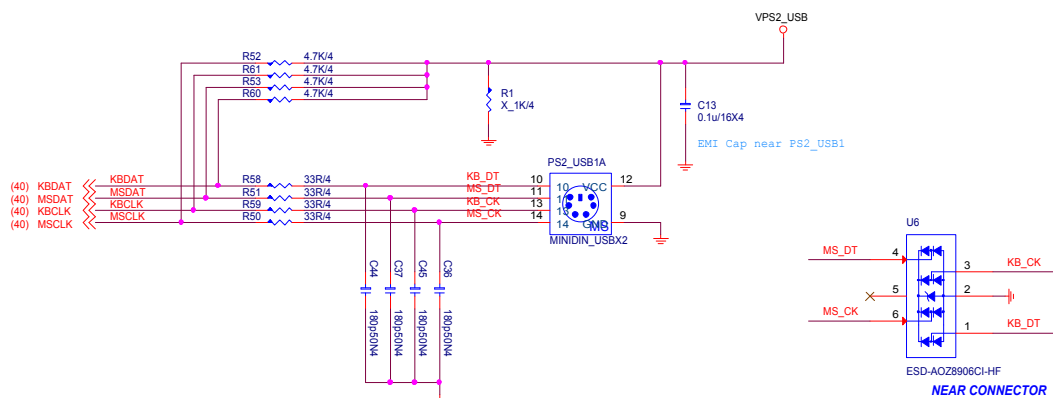


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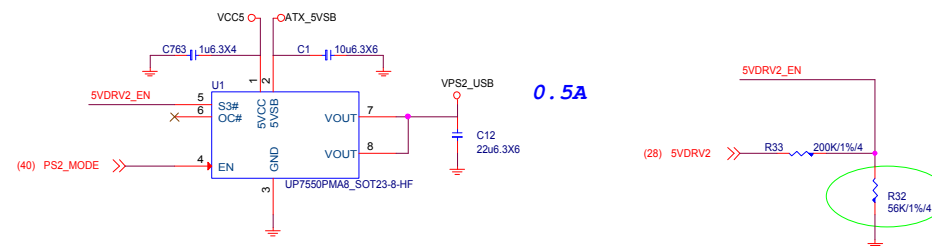
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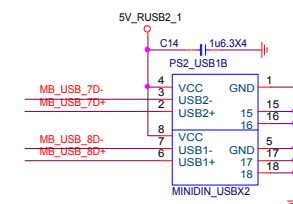
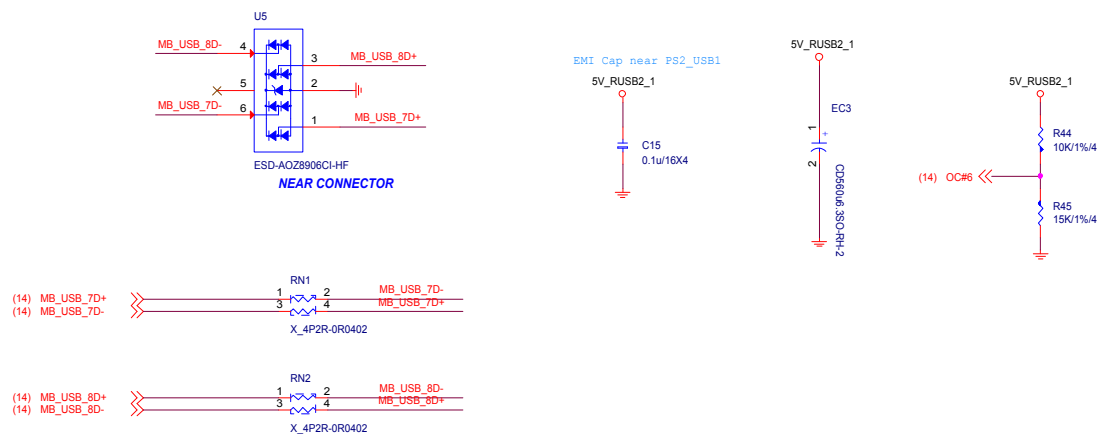
PS2 Connector



USB MODE



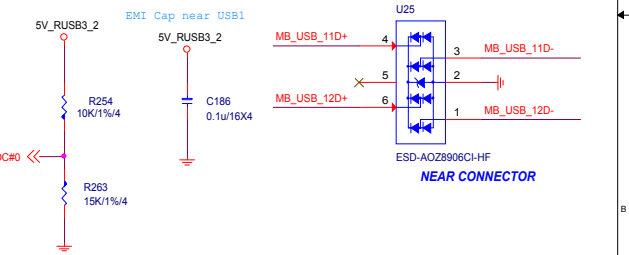
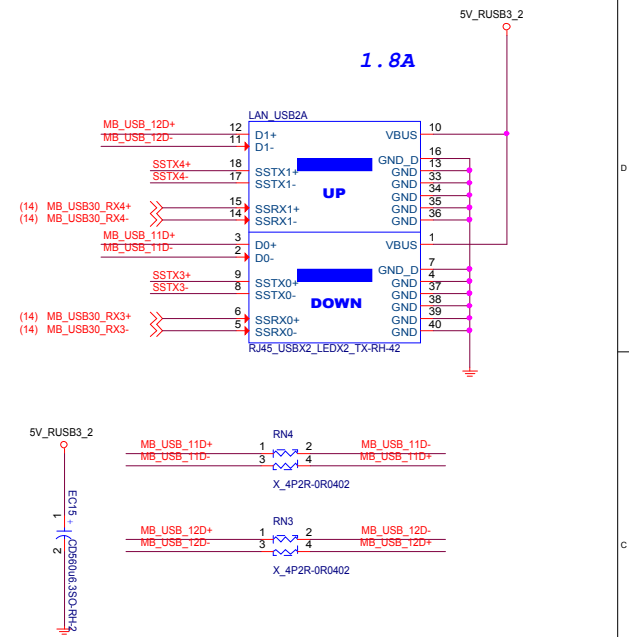
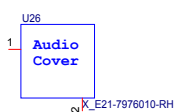
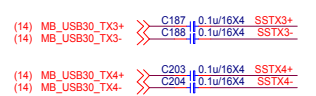
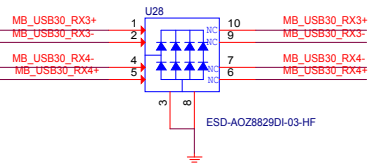
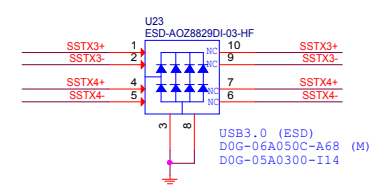
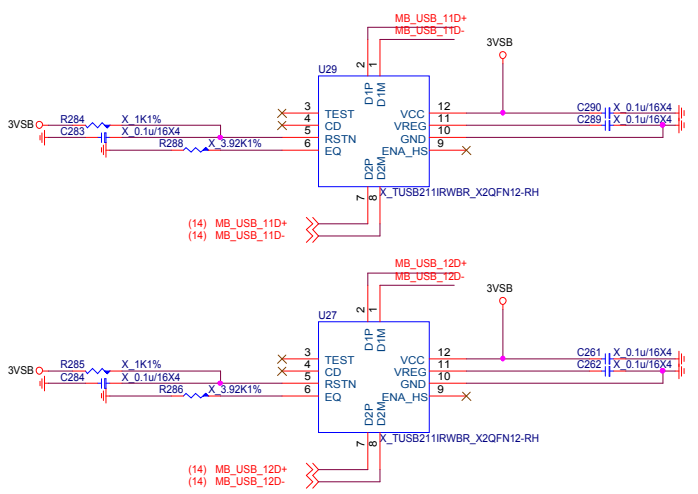
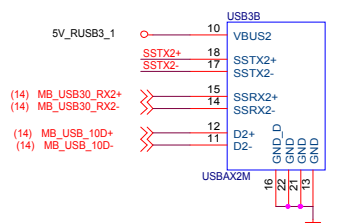
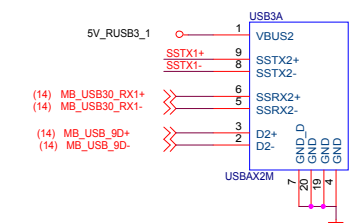
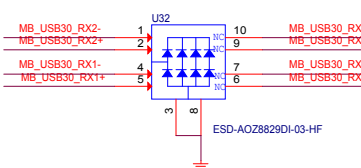
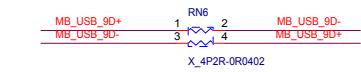
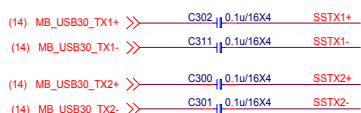
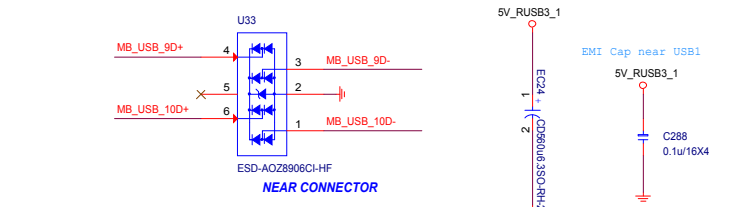
PS2_USB



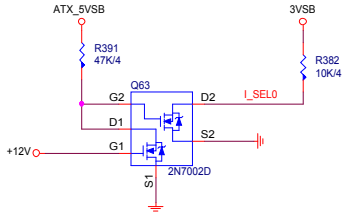
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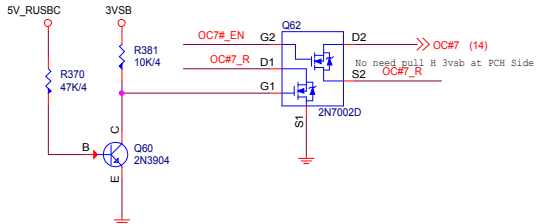
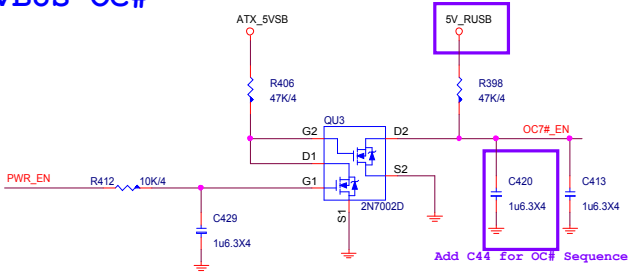
Current Mode



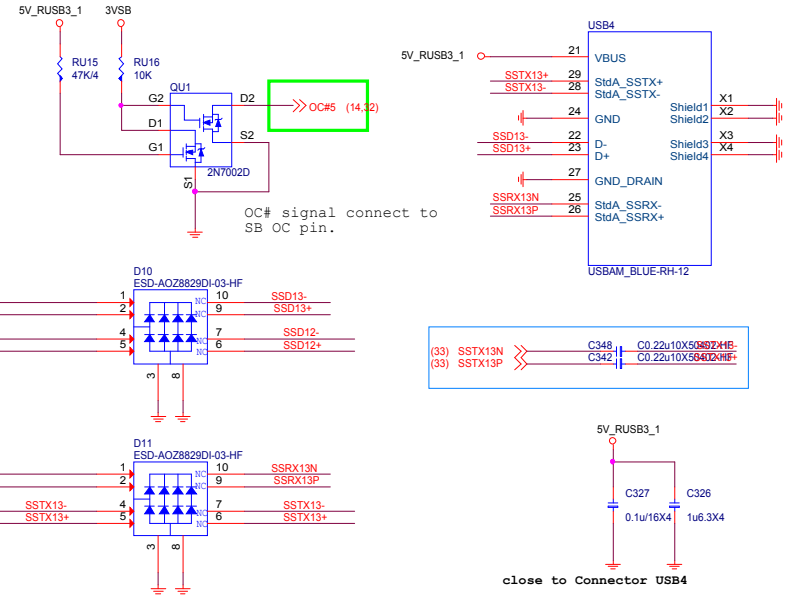
I_SEL0 : I_SEL1	
X 0	Default for 900mA
0 1	1.5A @5V
1 1	3A @5V

1.5A under S3 mode
3A under S0 mode

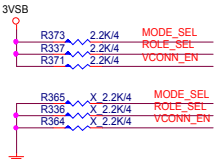
VBUS OC#



TYPE-A



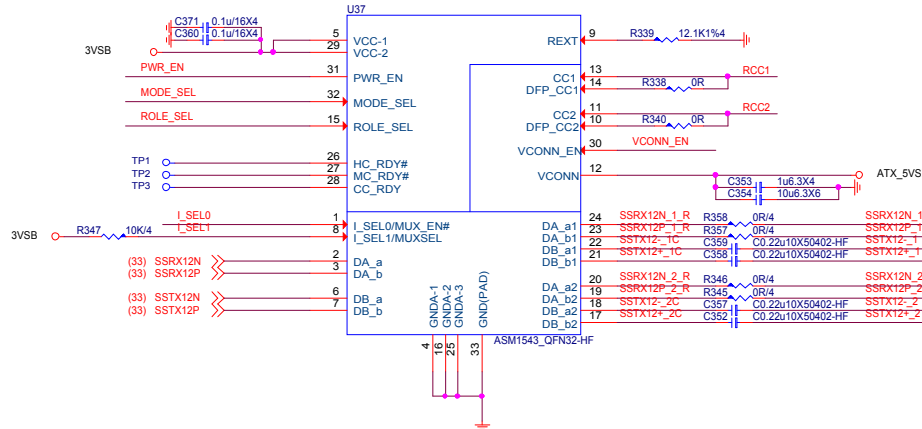
USB Type-C MUX with Configuration Channel (CC)



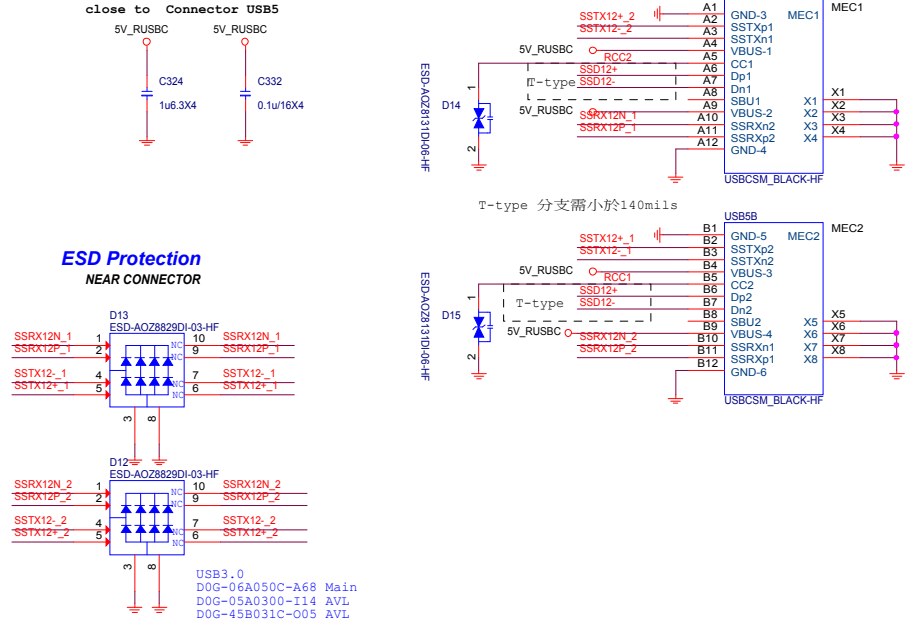
MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

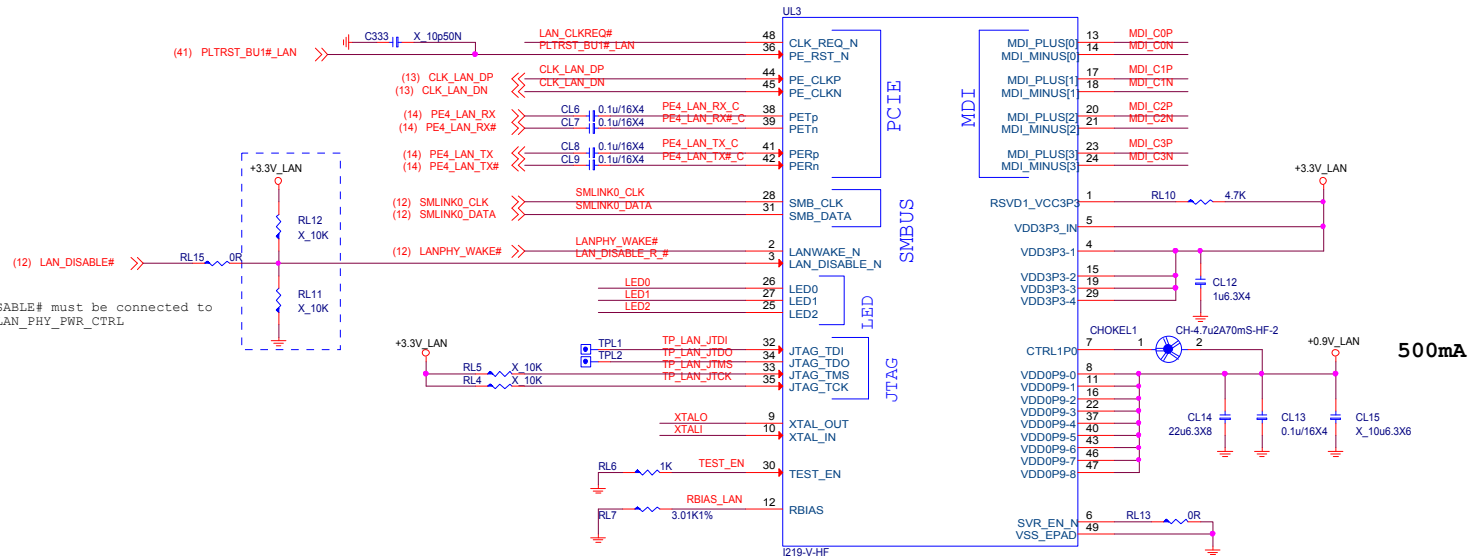
VCONN_EN	
1	enable
0	disable



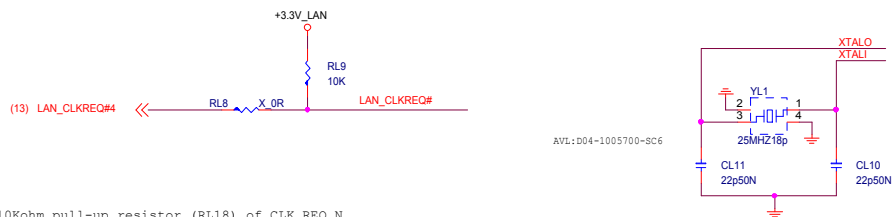
TYPE-C



8111H:B06-08111CC-R09
8111G:B06-081116C-R09

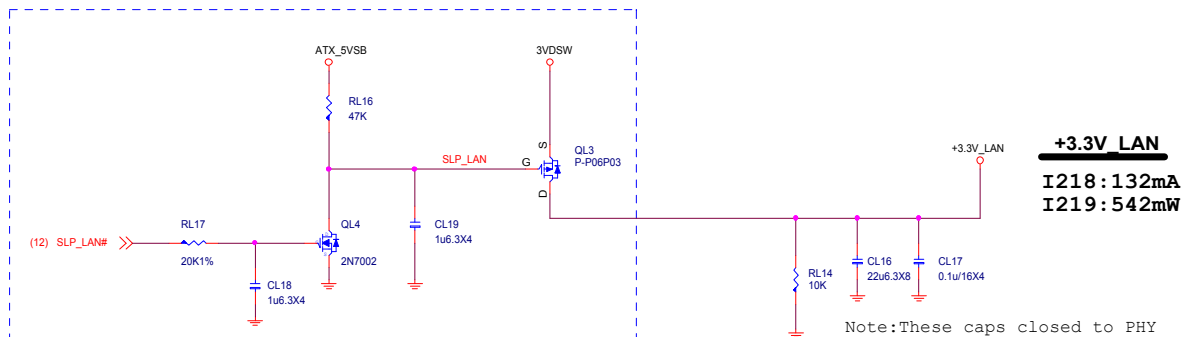


PCH's PCIECLKRQ<n> port must be mapped to PCH's PET/R<n+1>port.
If CLK_REQ_N is not used, pin48 is pulled up 10KR to 3.3V_LAN

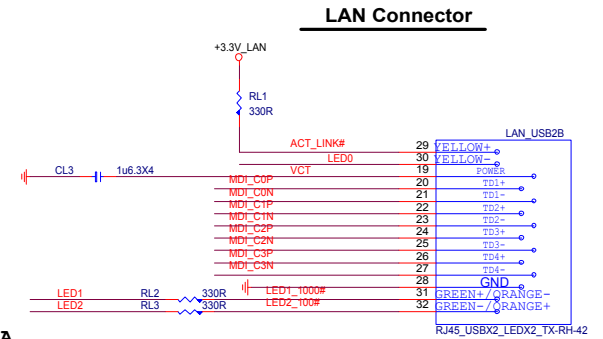


The 10Kohm pull-up resistor (RL18) of CLK_REQ_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIECLKRQ<n> buffer.

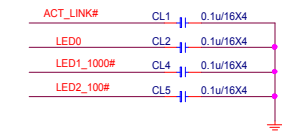
support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.



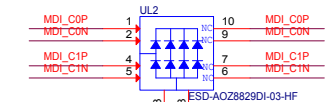
Note: These caps closed to PHY



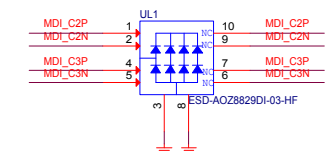
For EMI



UL2&UL3 close to connector



D0G-06A050C-A68
D0G-05A0300-I14



Do not pair MDIO and MDI1 on the same TVSdevice
(avoid LAN POE connecting issue).
Otherpairing combination is ok.

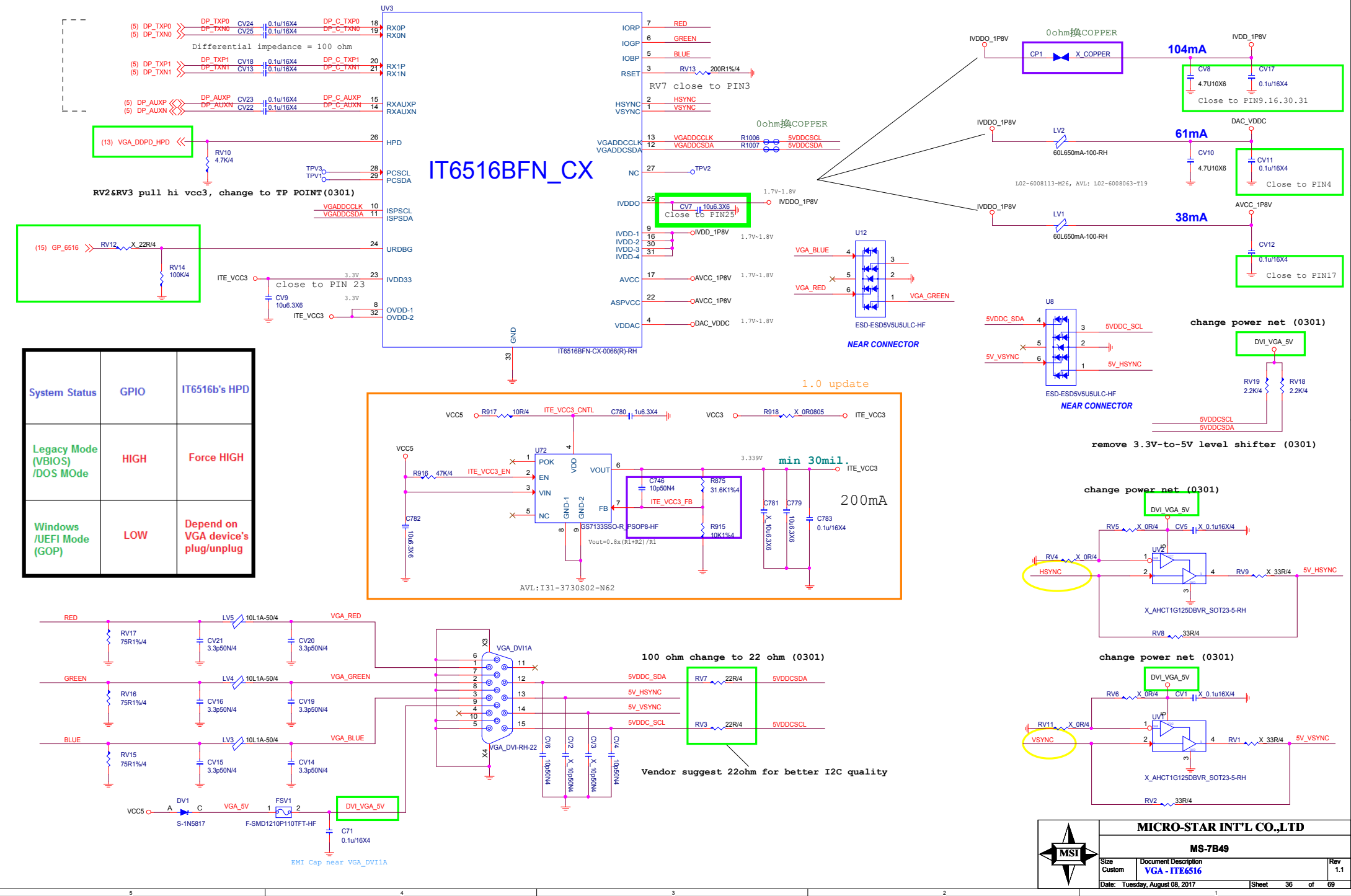


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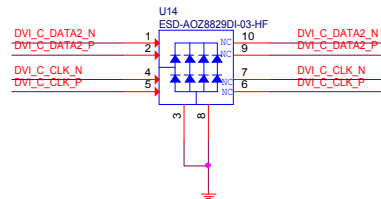
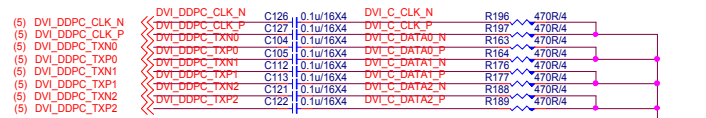
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Note:
If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining

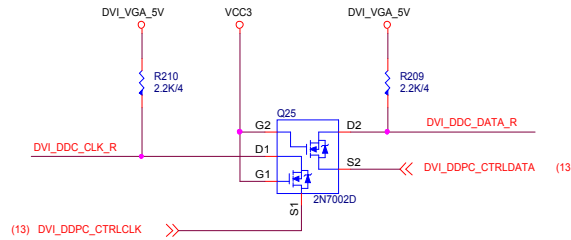
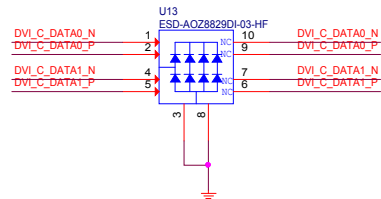


VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

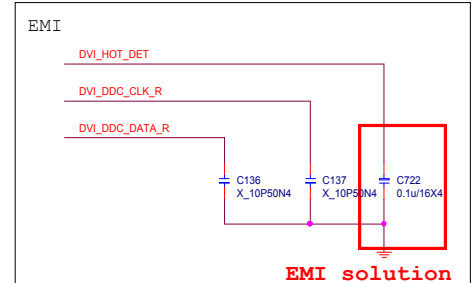
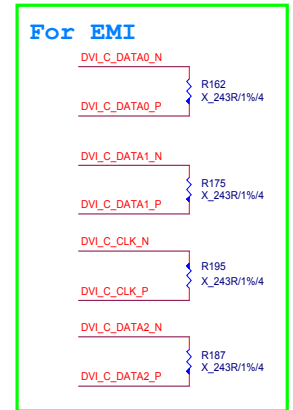
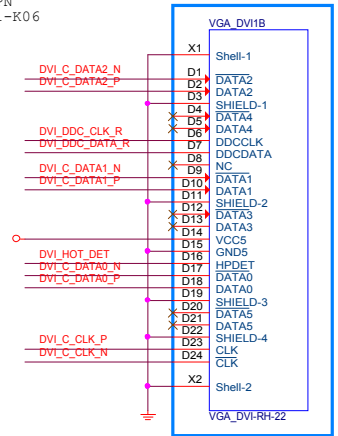
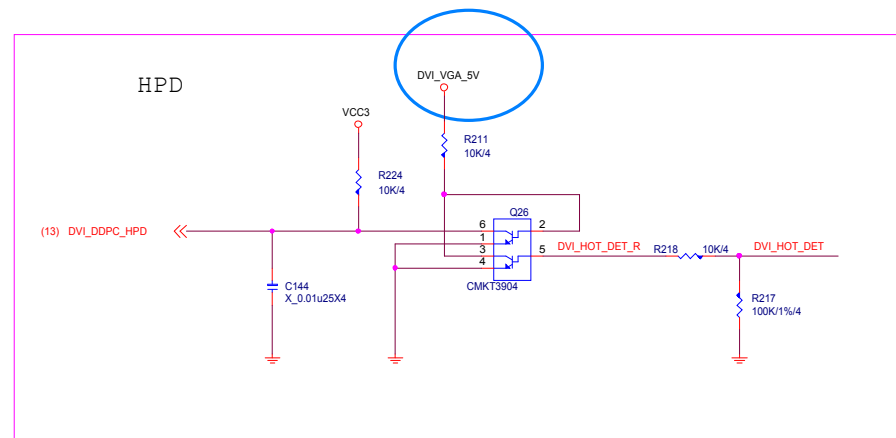
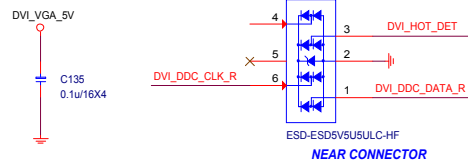
Check MSI PN
N58-39F0231-K06



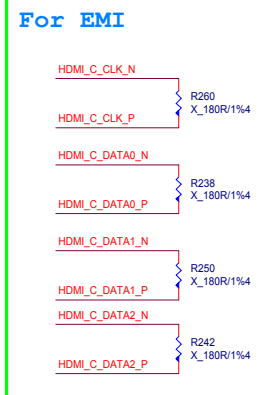
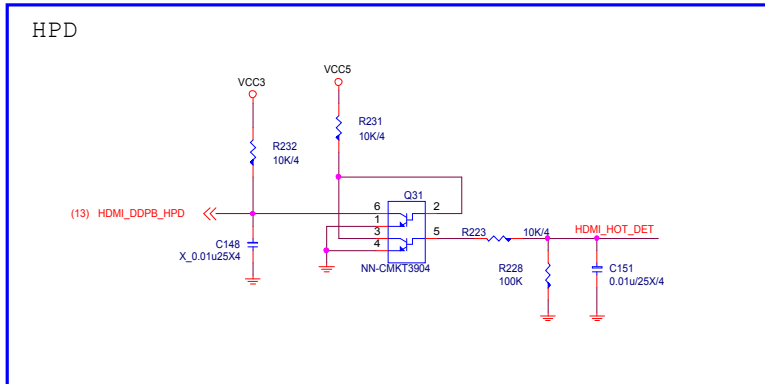
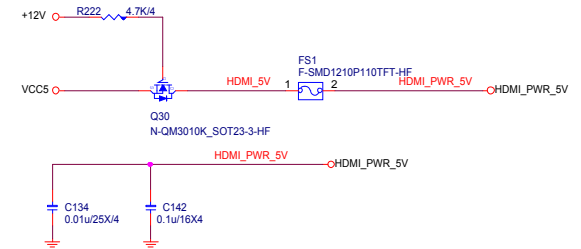
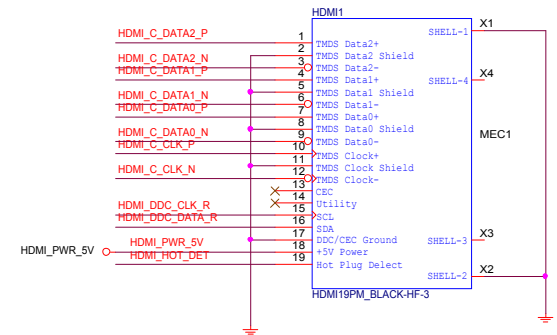
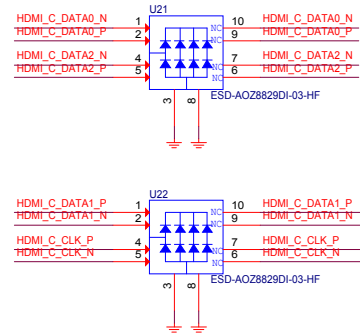
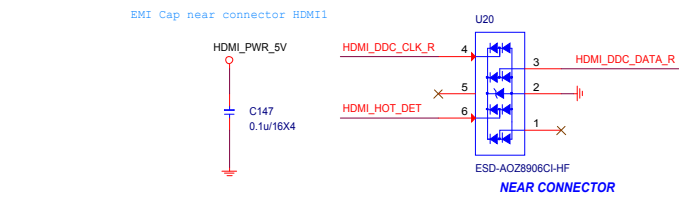
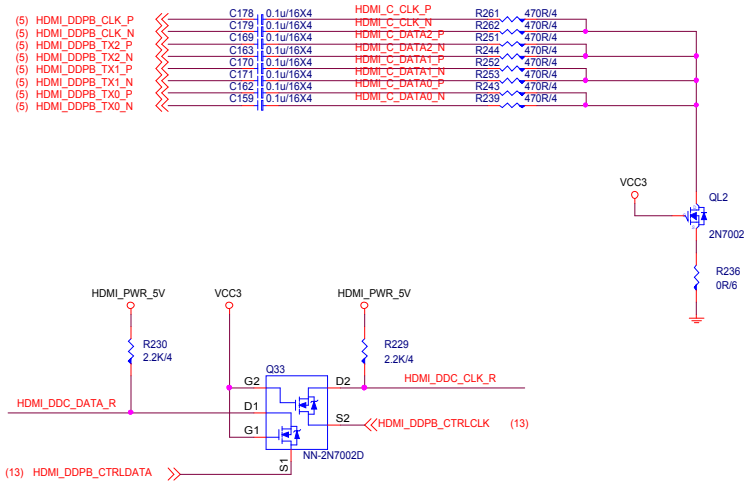
U27 AVL:D0G-05A050C-005
D0G-06A050C-A68



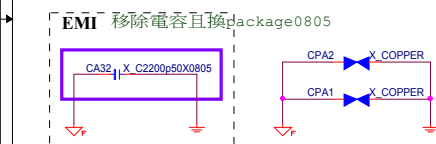
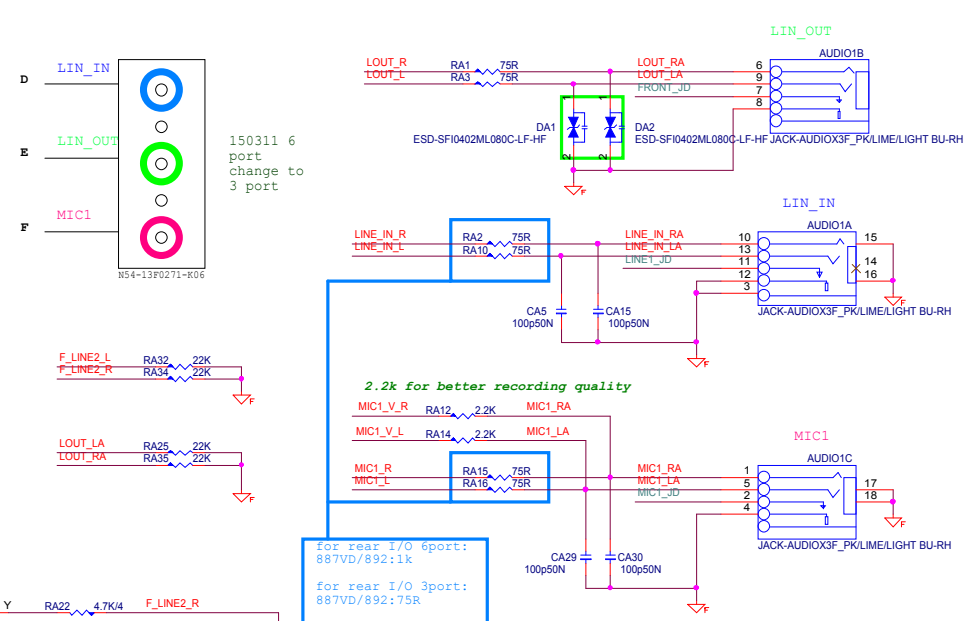
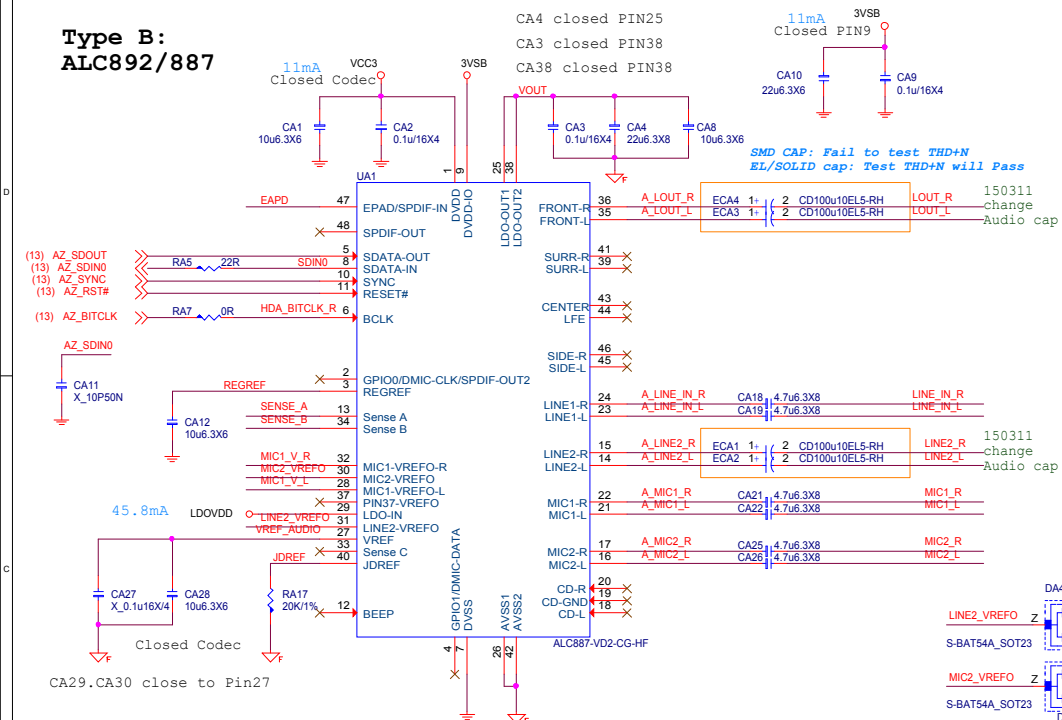
EMI Cap near connector DV11



HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

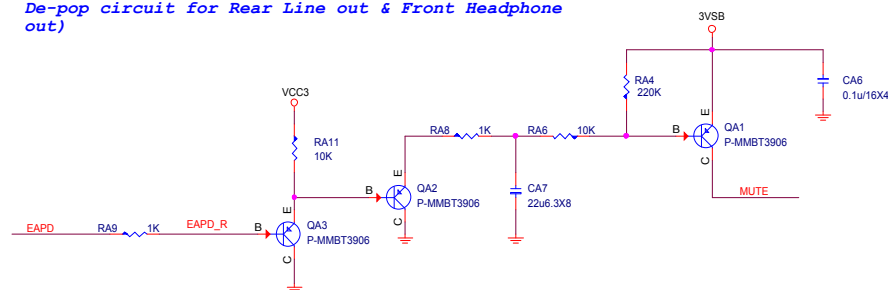
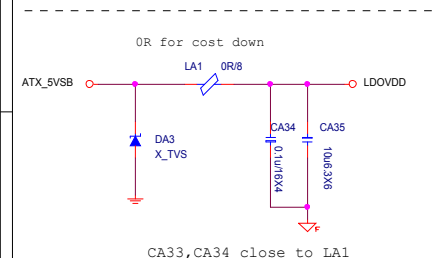


Type B:
ALC892/887



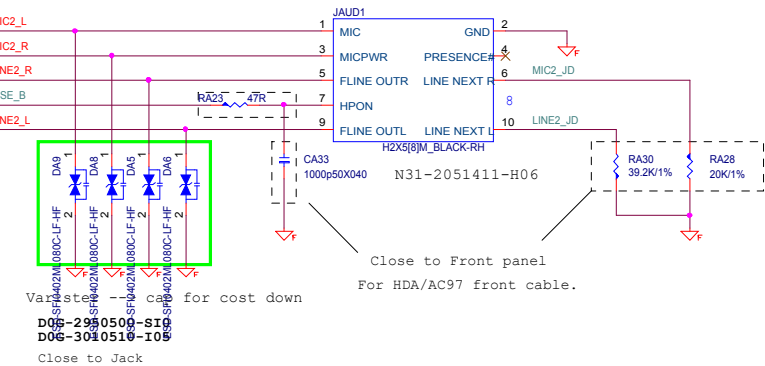
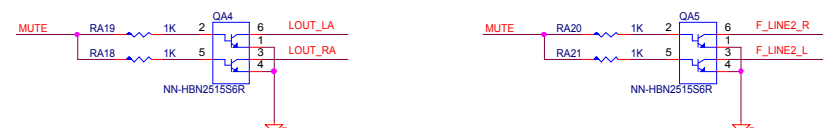
Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)



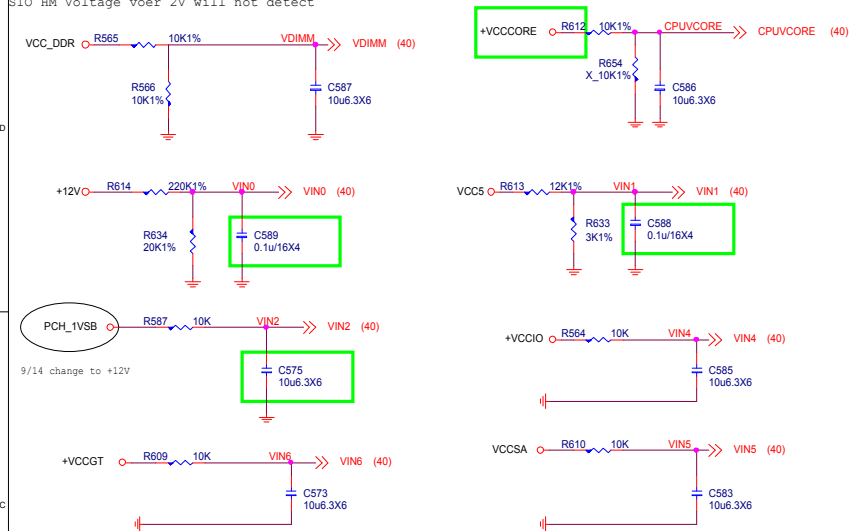
Digital

Analog

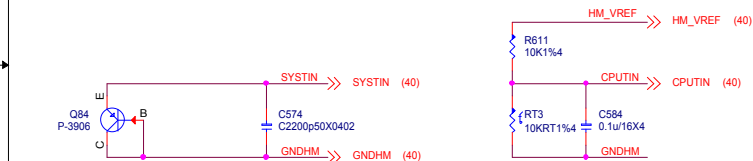


HW Monitor - Voltage

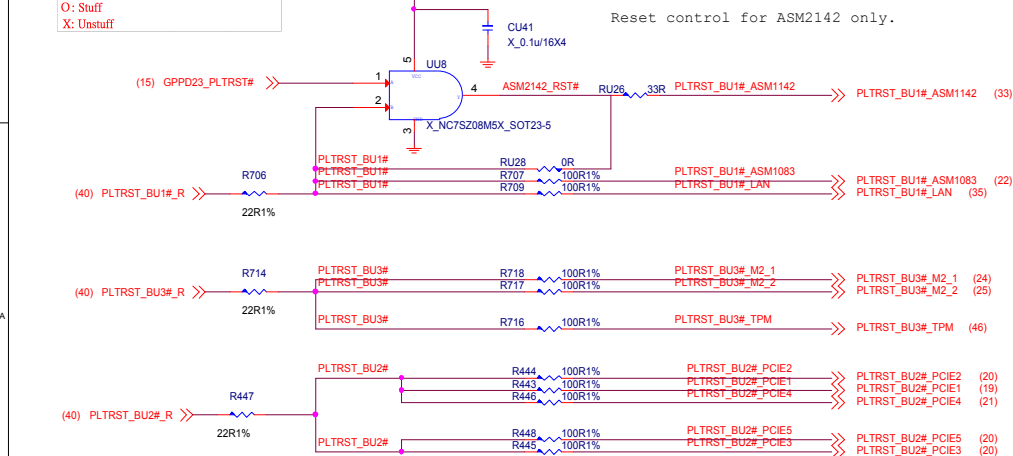
SIO HM Voltage voer 2V will not detect



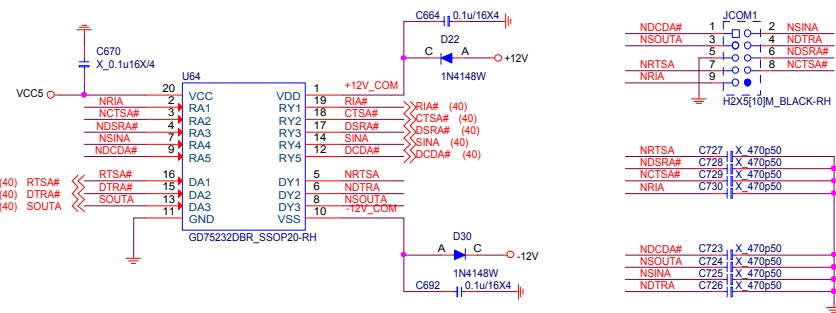
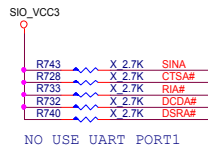
Thermal Monitor



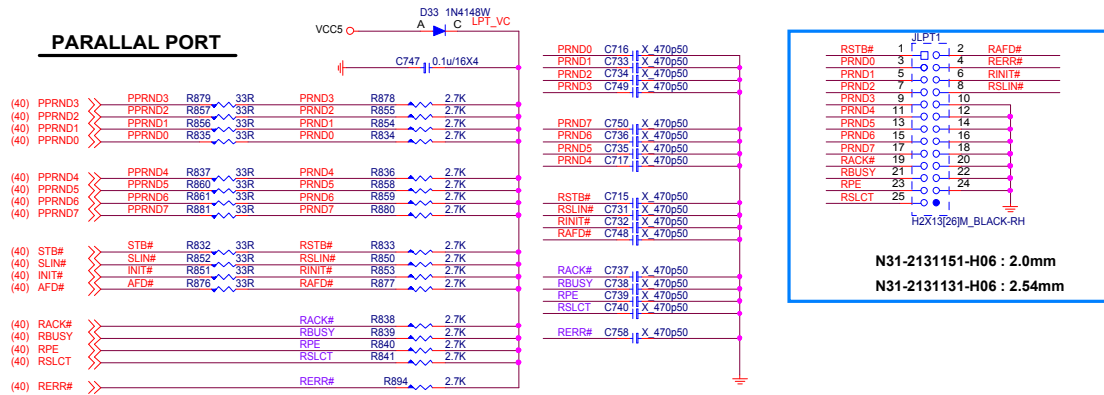
	U18	RU6	CU39
ASM2142	O	X	O
ASM3142	X	O	X
O: Stuff			
X: Unstuff			



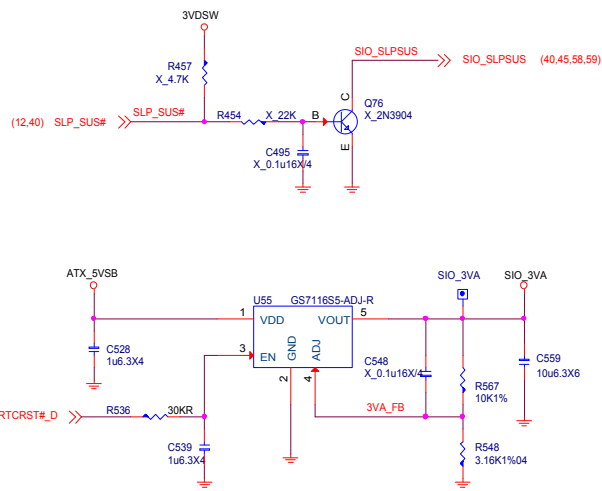
SERIAL PORT 1



PARALLAL PORT

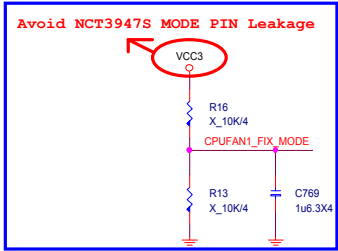
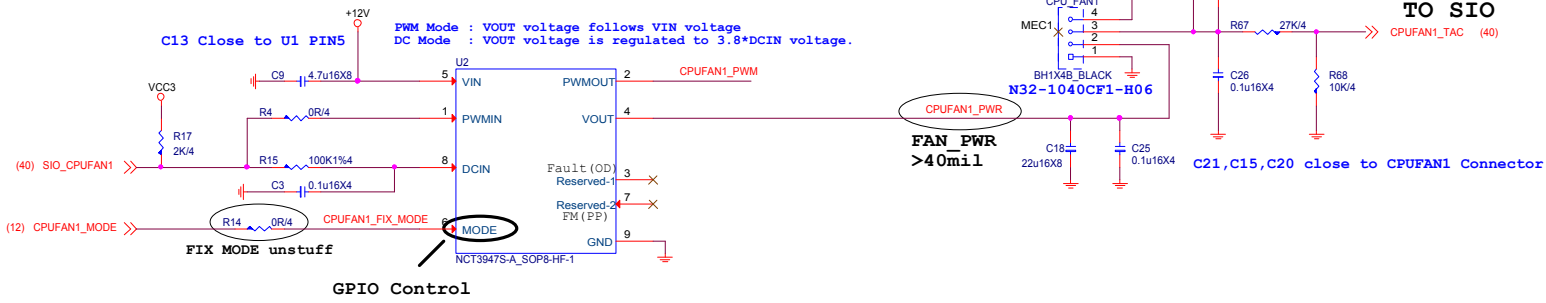


SLP_SUS Co-lay circuit



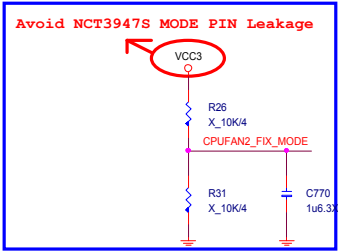
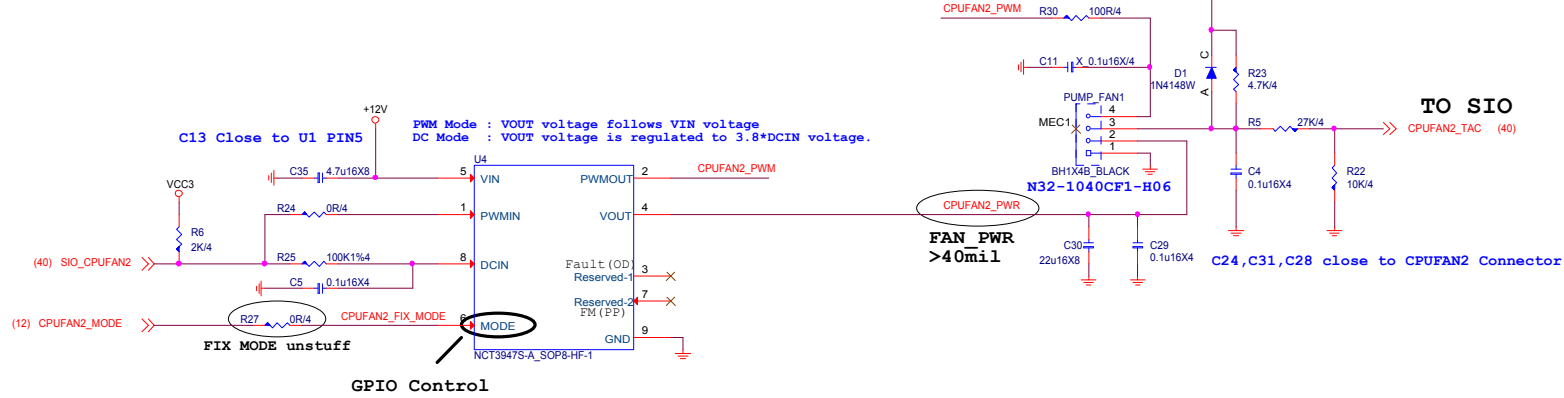
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

- 1. PWM/DC/OCF LED (現在是改成R/G/B3色LED)
- 2. GPIO可以由BIOS切換 PWM/DC MODE
- 3. OCP拉回GPIO給BIOS認
- 4. PWM OR DC FAN拉回GPIO給BIOS認
- 5. FAN轉速加快的時候由SOFTWARE 控制GPIO讓燈的變化



Resever For FIX DC or PWM MODE USE By PM SPEC

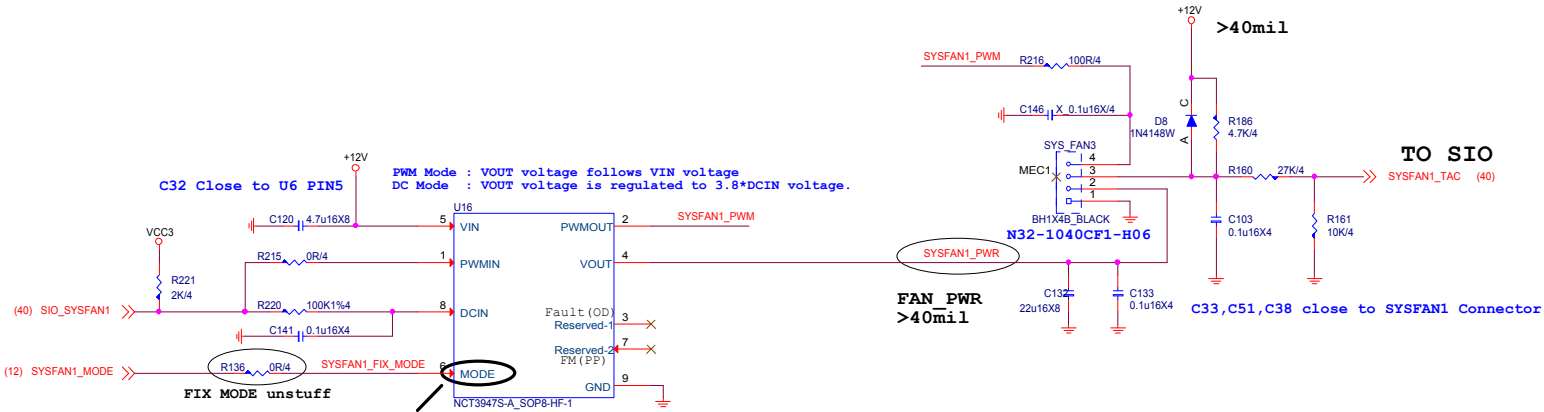
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



Resever For FIX DC or PWM MODE USE By PM SPEC

- 1. MODE : USE MODE PIN change FAN MODE (PWM or DC FAN)
- 2. FAULT : USE FAULT PIN Triger OVT/OCF Protection, LOW Atcive (Reserve NEW IC)
- 3. FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information (Reserve NEW IC)

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

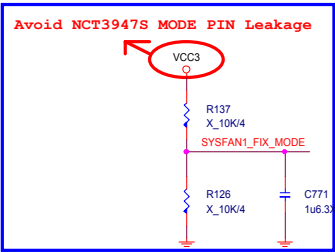


GPIO Control

	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

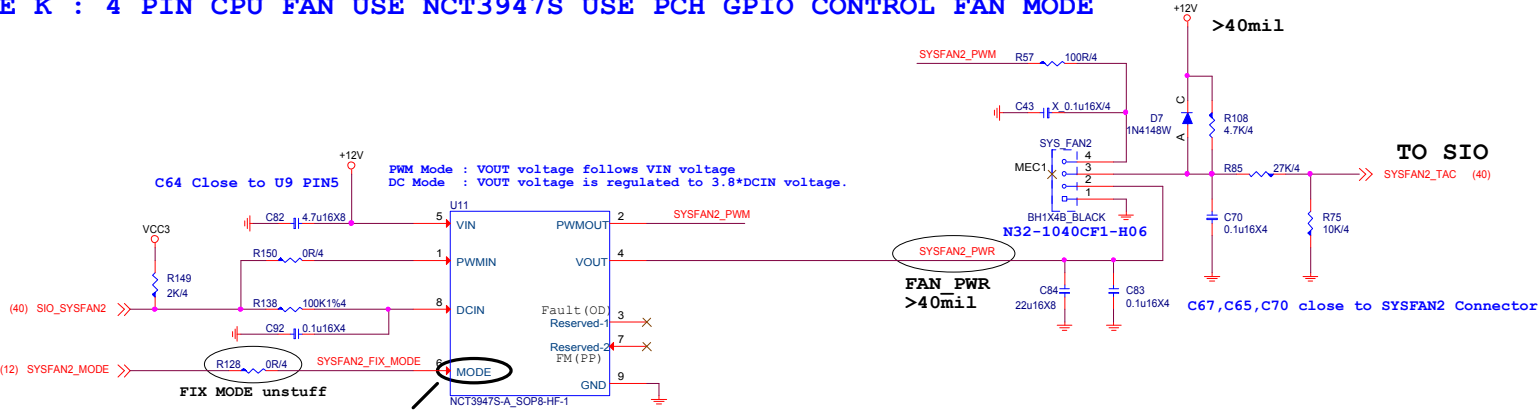
Default

Internall pull up 1.65V



Resever For FIX DC or PWM MODE USE By PM SPEC

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

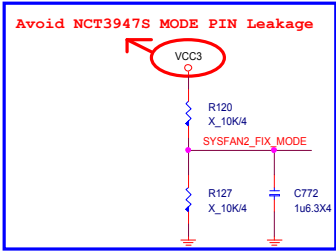


GPIO Control

	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Default

Internall pull up 1.65V



Resever For FIX DC or PWM MODE USE By PM SPEC

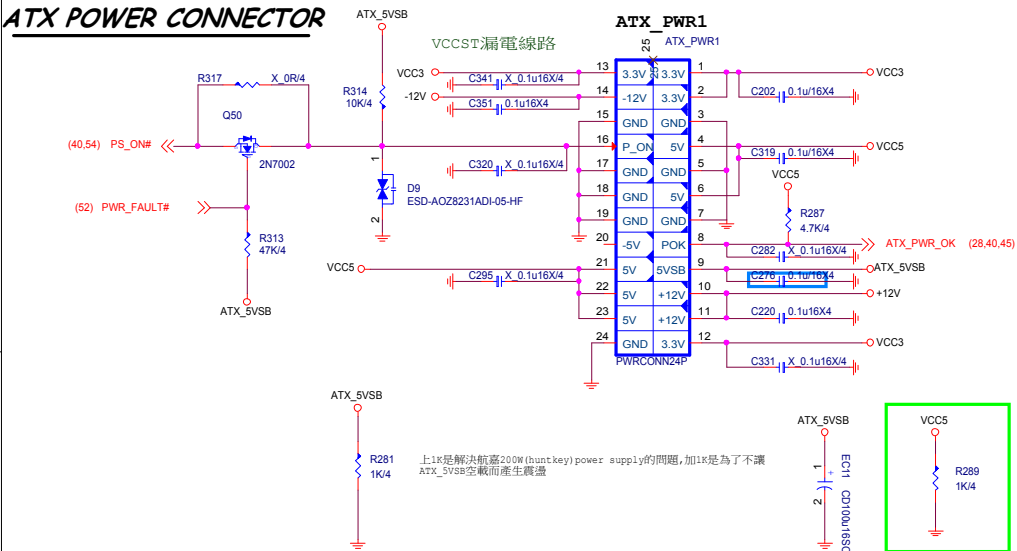


MICRO-STAR INT'L CO.,LTD

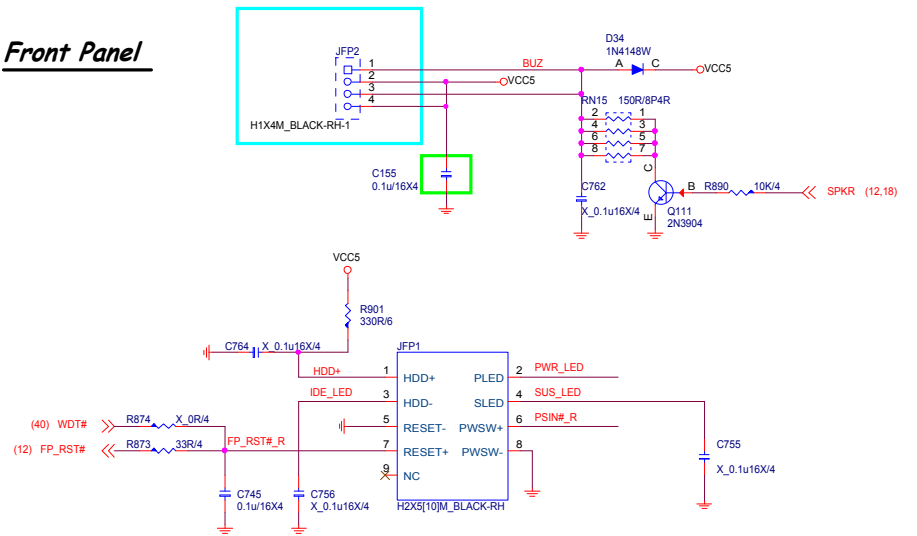
MS-7B49

Size	Document Description	Rev
Custom	SYSTEM FAN 1/2	1.1
Date:	Tuesday, August 08, 2017	Sheet 43 of 69

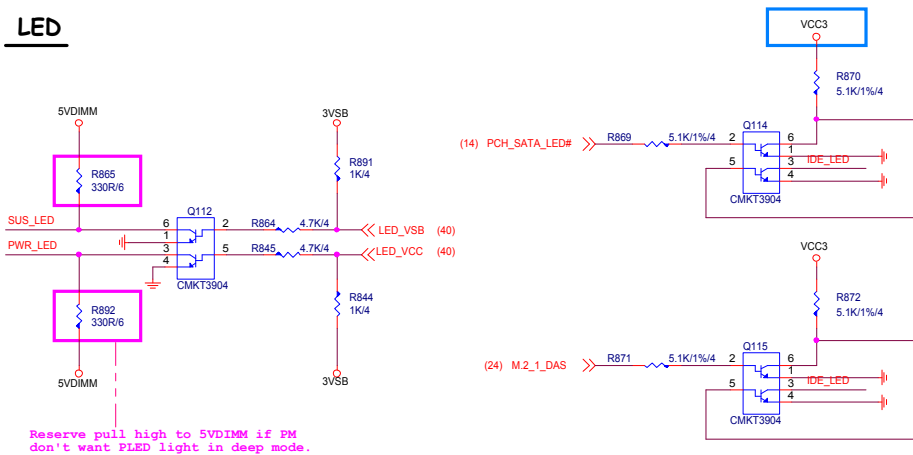
ATX POWER CONNECTOR



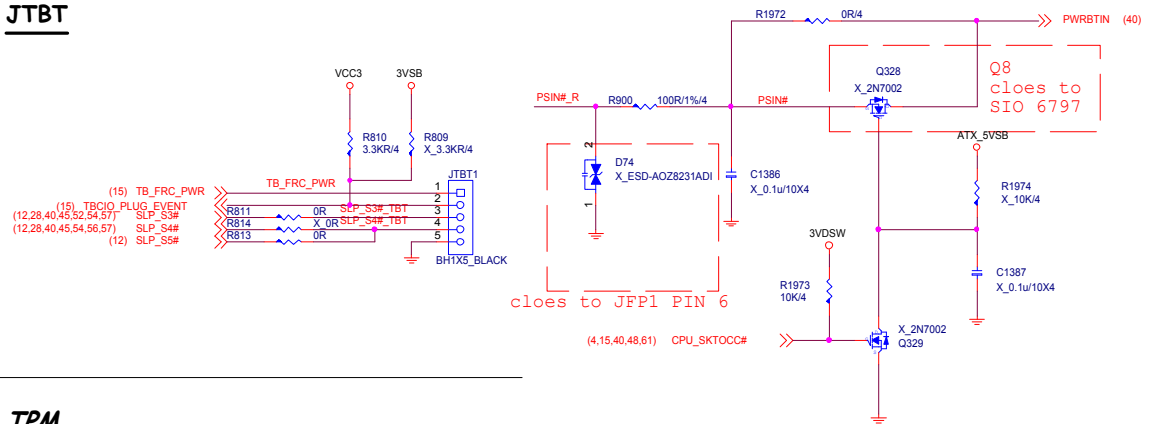
Front Panel



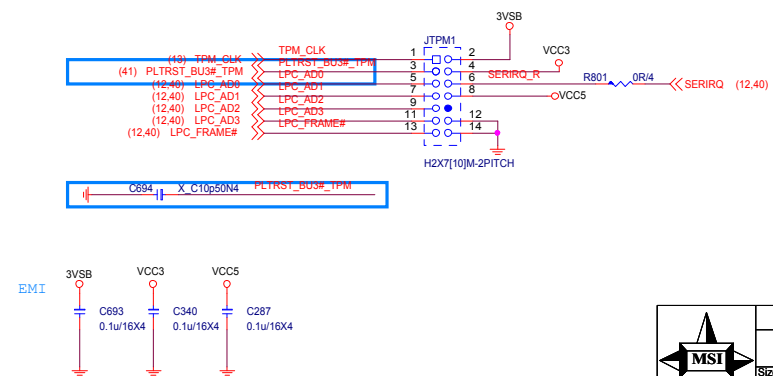
LED



JTBT



TPM



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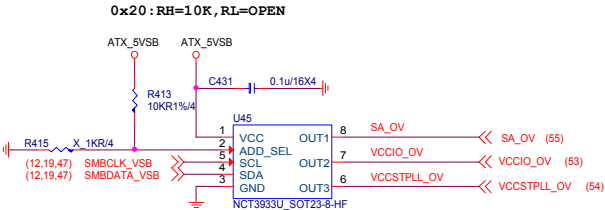
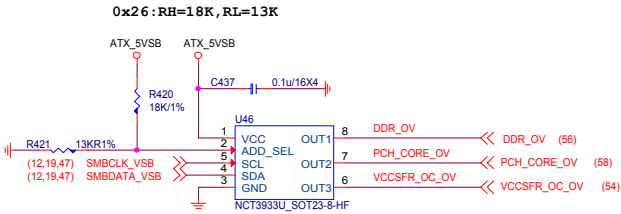
MS-7B49

Size Custom	Document Description ATX Power/F_Panel	Rev 1.1
Date: Tuesday, August 08, 2017	Sheet 46 of 69	

Over Voltage Control IC

UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

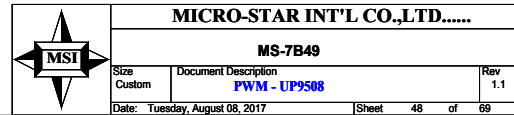
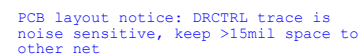


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Size	Document Description	Rev
Custom	OV-NCT3933/GPIO-NCT5605	1.1
Date:	Tuesday, August 08, 2017	Sheet 47 of 69

VGT: ICC Max 45A
LL: 3.1 mohm
OCP: 75A

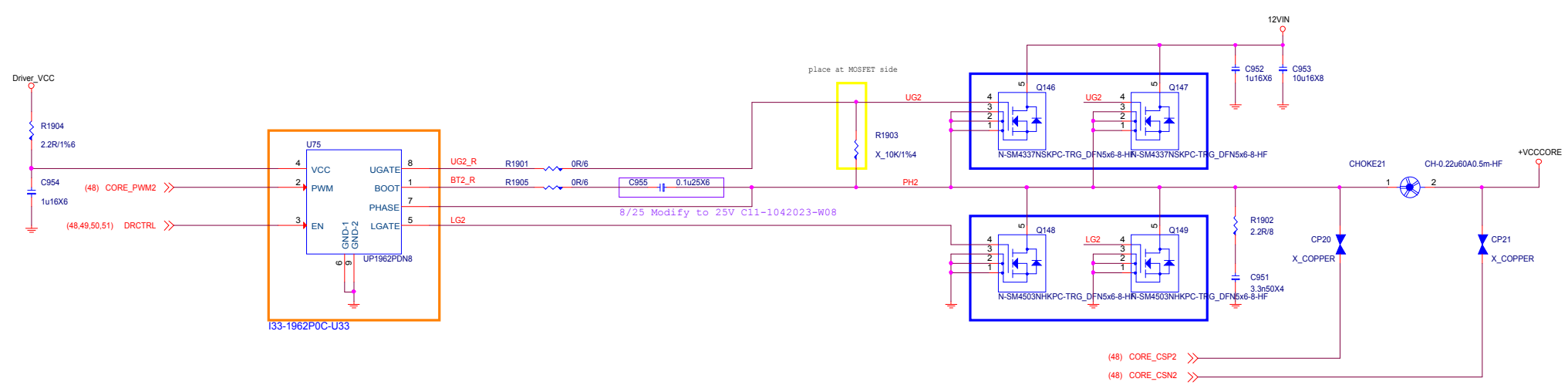
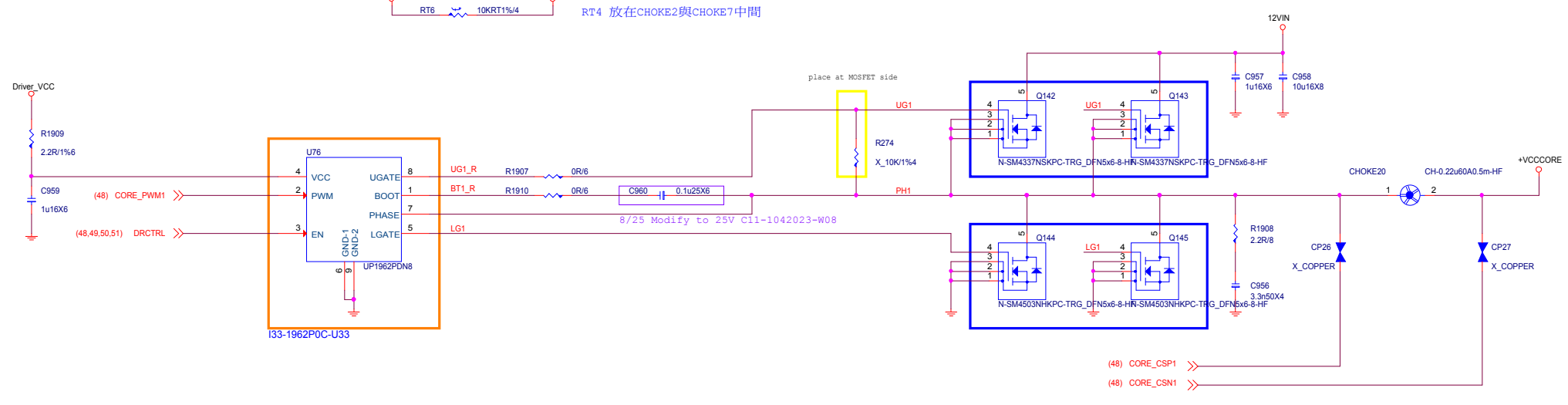


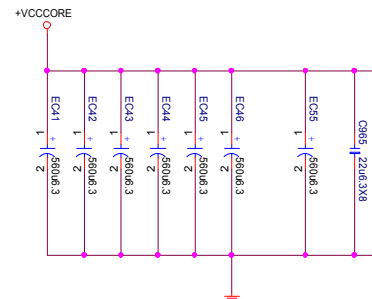
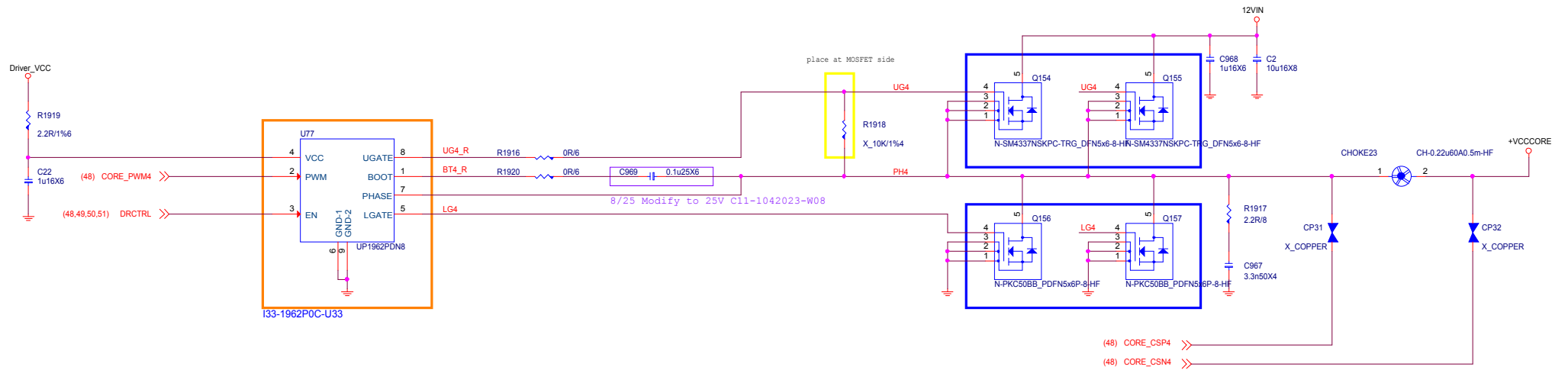
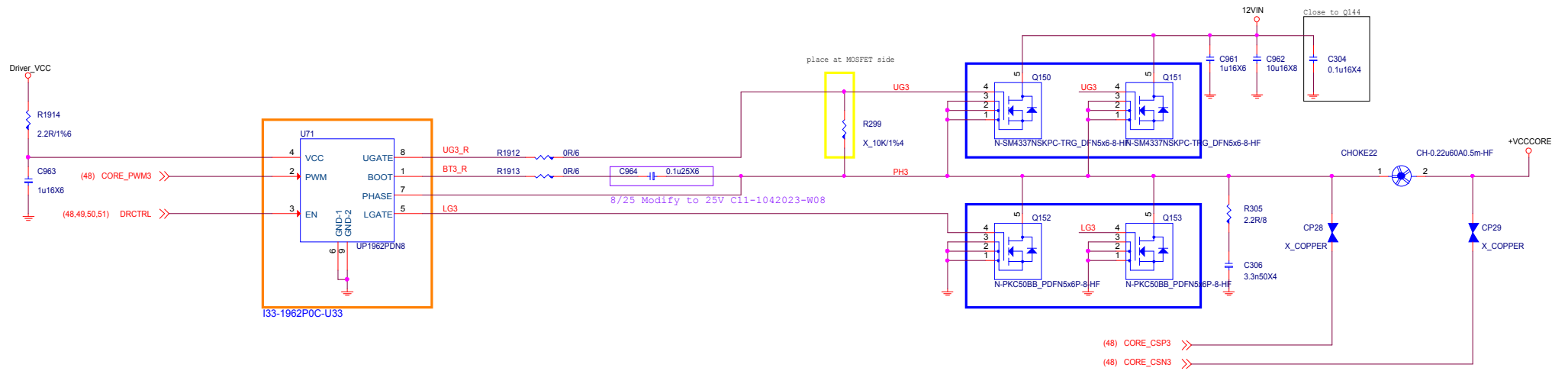
12VIN R1900 0R/6
+12VIN R1899 X_0R/6 Driver_VCC

NTC1a RT7 100KRT1%4
NTC1b RT6 10KRT1%4
NTC1c RT4 10KRT1%4

RT3放置在VccCORE 這組switching power 最熱的地方
RT4 放在CHOKE2與CHOKE7中間

Vcore = 1.52V
ICCMAX = 138A
Irms = 17.25A

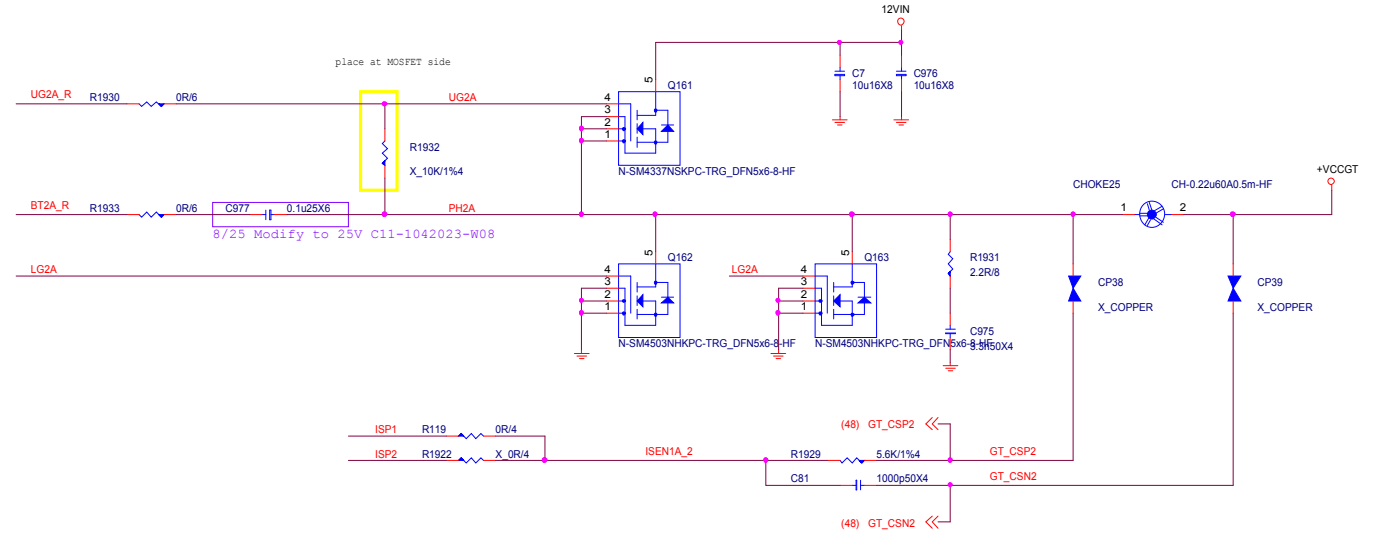
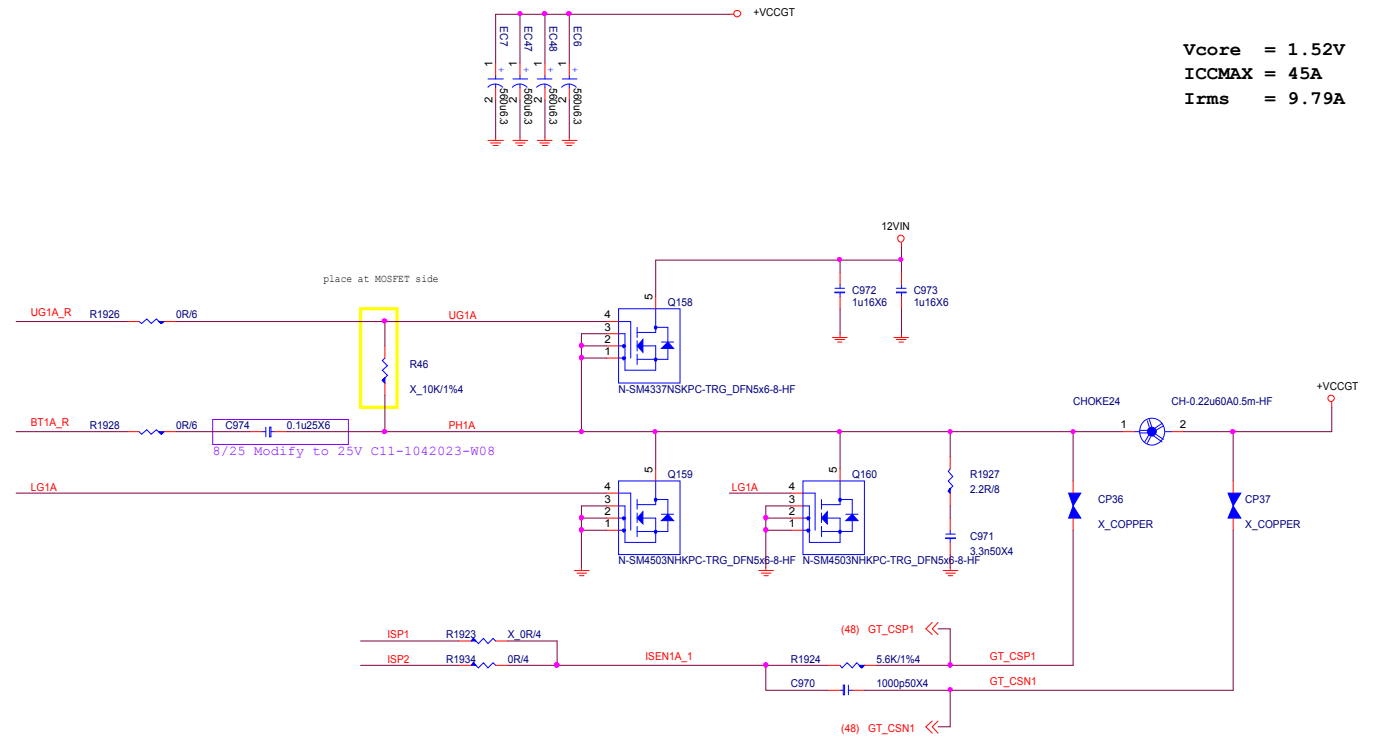
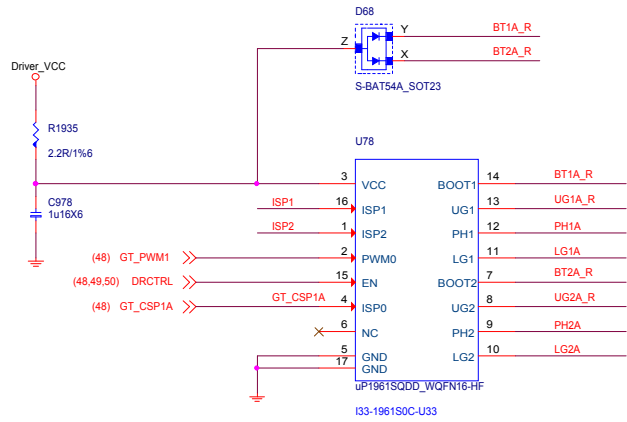
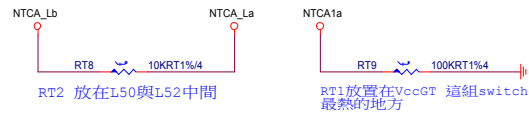




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Size	Document Description	Rev
Custom	VCORE - PHASE 2-4	1.1
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Vcore = 1.52V

ICCMAX = 45A

Irms = 9.79A

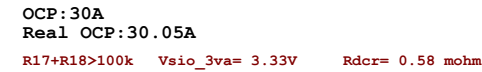
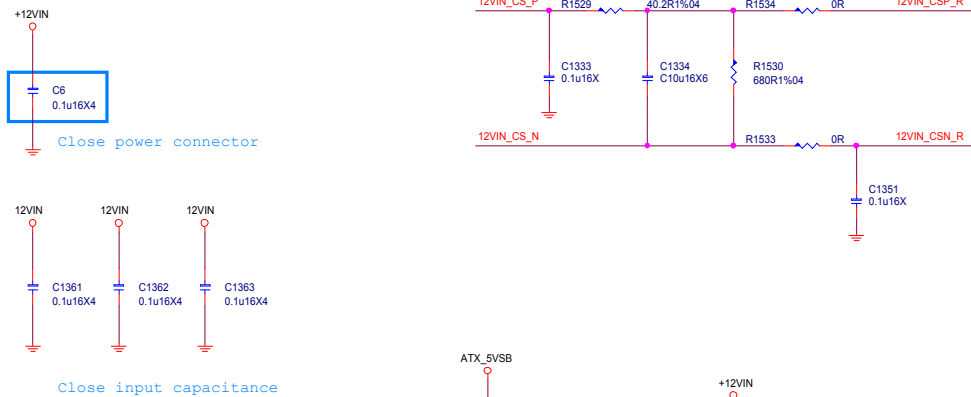


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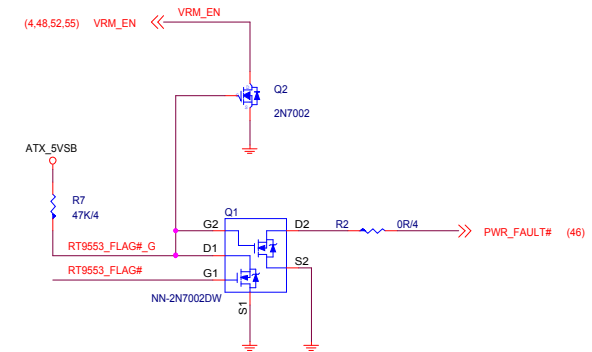
MS-7B49

Size	Document Description	Rev
Custom	VGT - PHASE 1-2	1.1
Date: Tuesday, August 08, 2017	Sheet 51 of 69	

```
Iripple = 27.04A
VCORE   = 17.25A
VGT      = 9.79A
```



```
I3933_imon*[R17*R18/(R17+R18)]= Istep* RdcR*100
I3933_imon= 10uA/step
Istep=4.785A
```

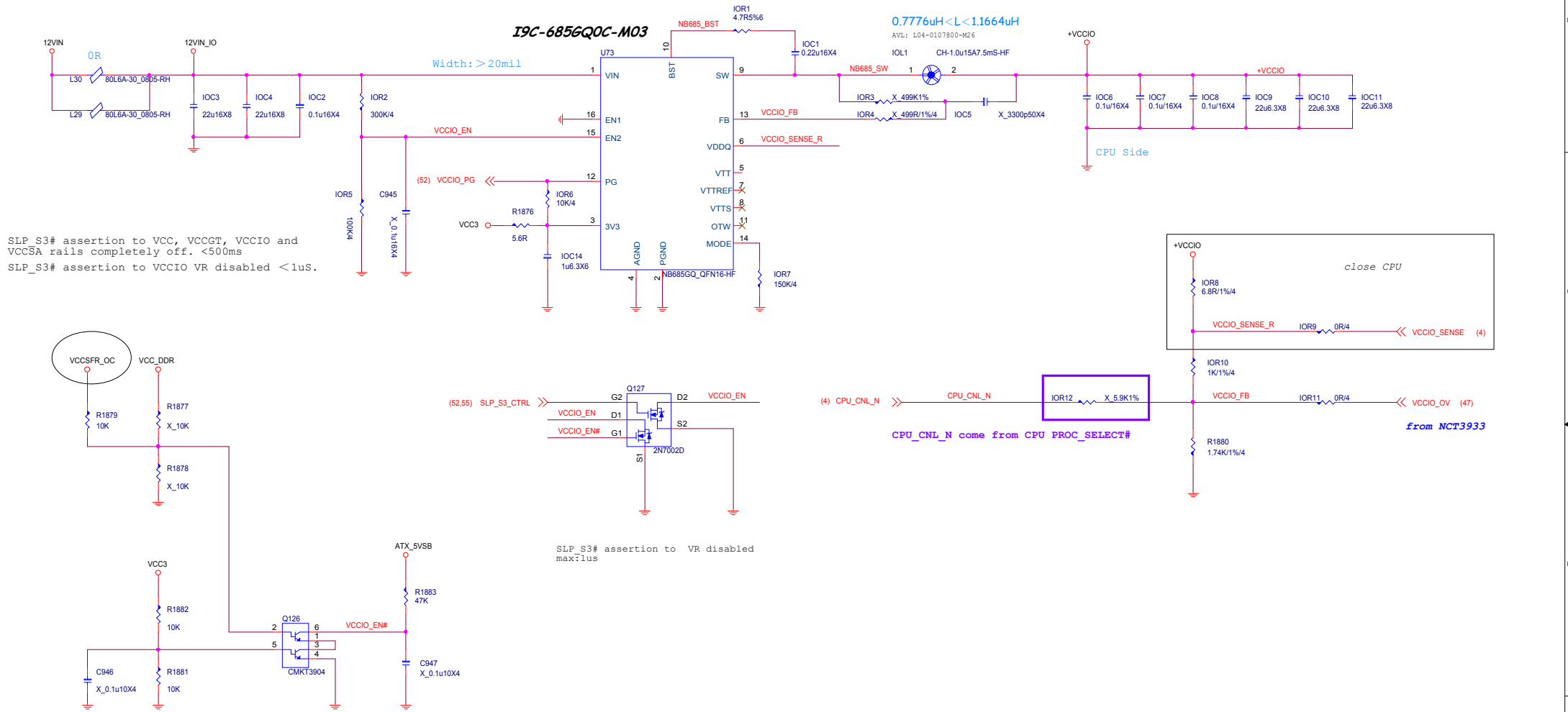


VCCIO

0.95V ; 6.4A

IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

support OV=>NB685



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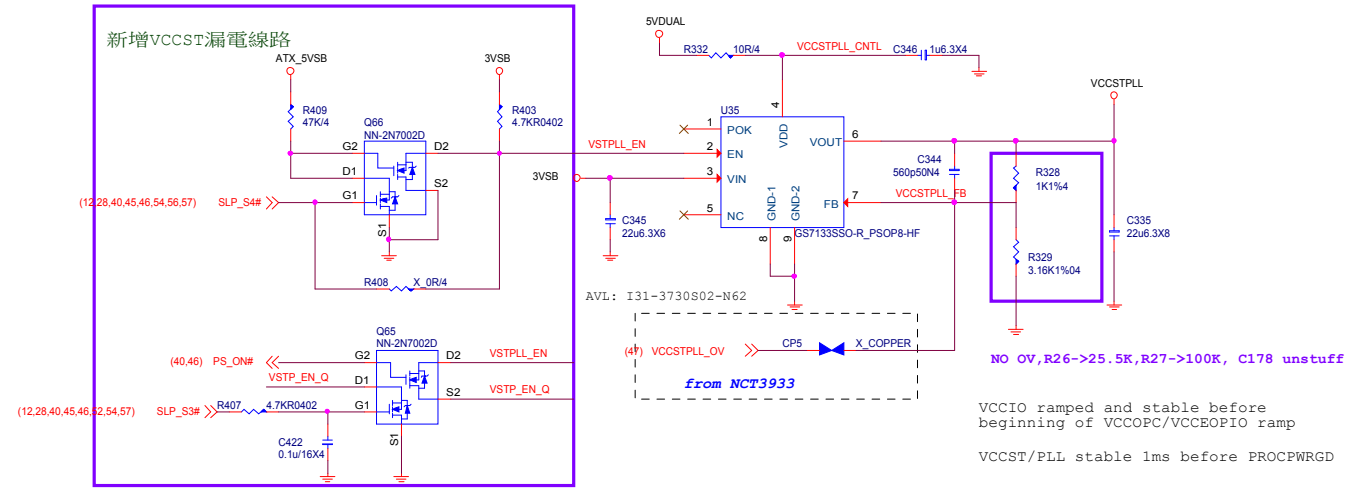
Size	Document Description	Rev
Custom	VCCIO - NB685	1.1
Date: Tuesday, August 08, 2017	Sheet 53 of 69	

VCCSTPLL

1.0V; 250mA

For Cost down VCCST&VCCPLL merge

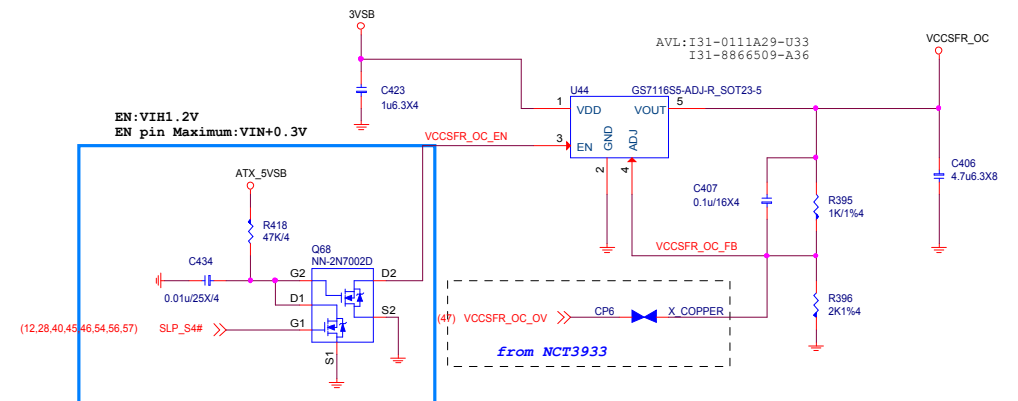
for Gaming3/5, Classic, ECO and H110



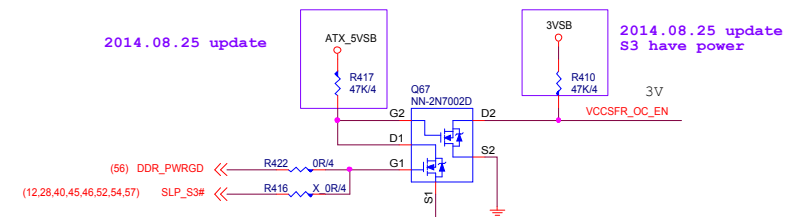
VCCPLL_OC

1.2V; 130mA

2014.08.21 update



2014.08.25 update



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Size	Document Description	Rev
Custom	VCCST/PLL - GS7133/7116	1.1
Date: Tuesday, August 08, 2017	Sheet 54 of 69	

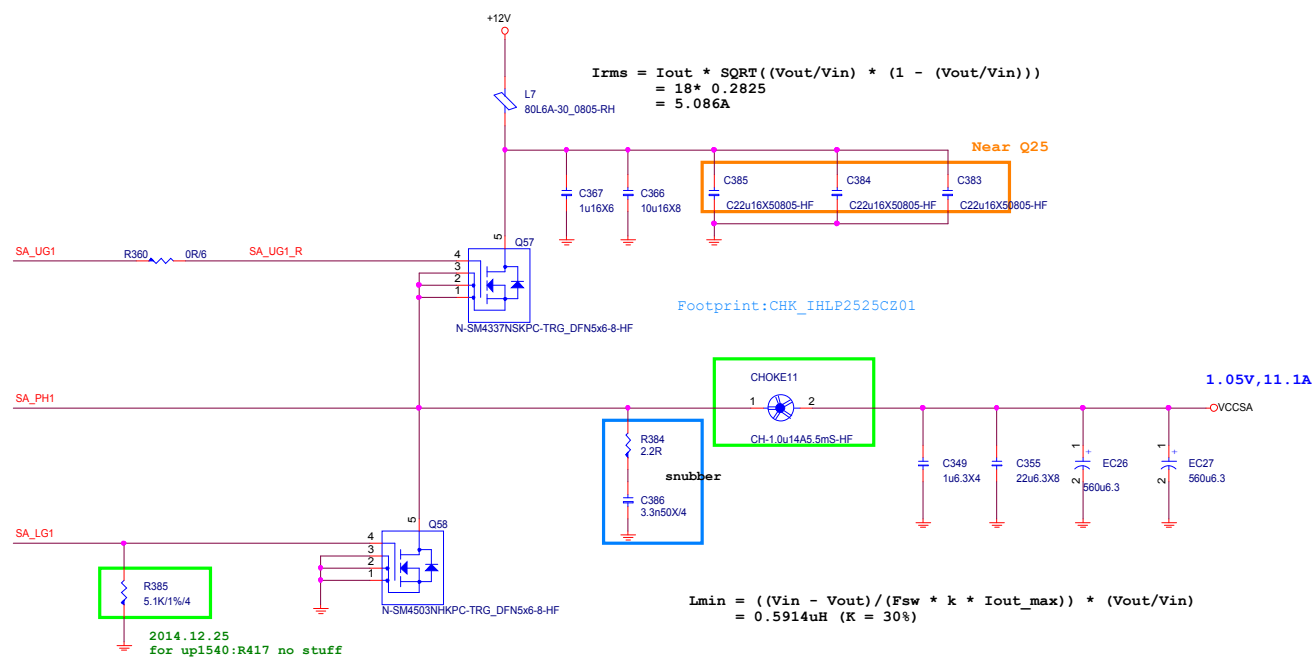
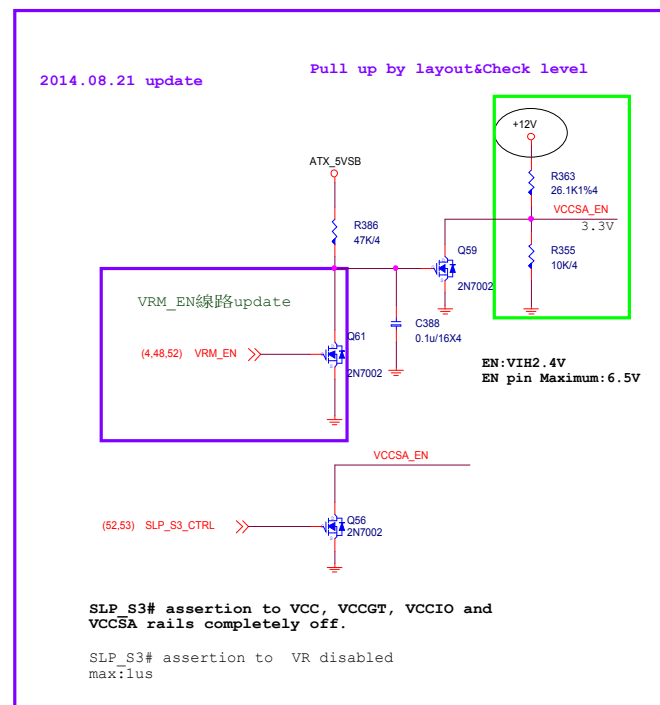
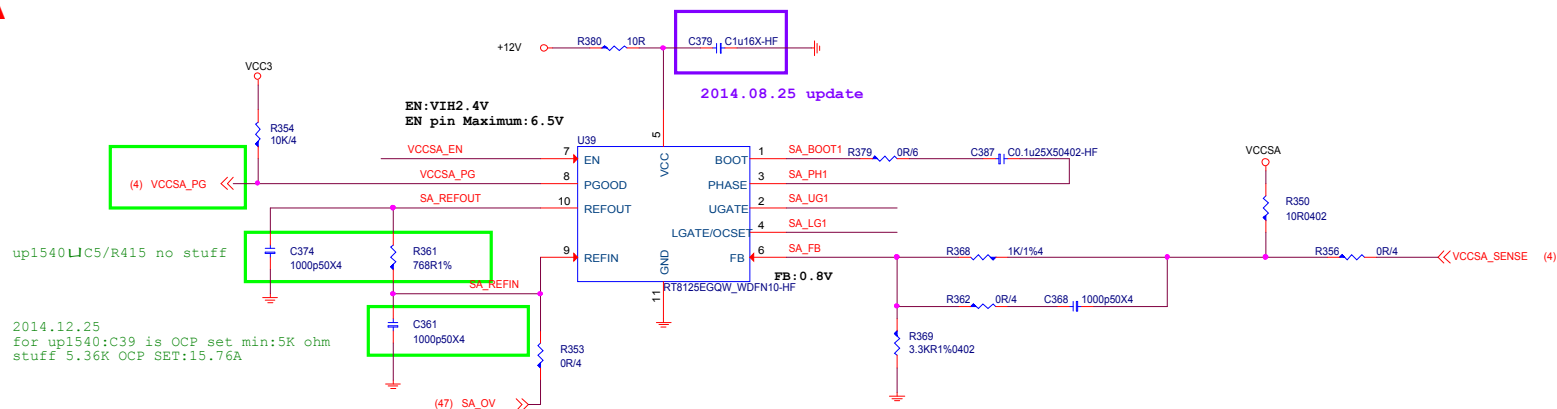
$$\begin{aligned} R_{ocpset} &= 5.6K \\ OCP &= R_{ocpset} * R_{dson}(\text{Low side}) / 10uA \\ &= 5.1K * 3mohm / 10uA \\ &= 19A \end{aligned}$$

```

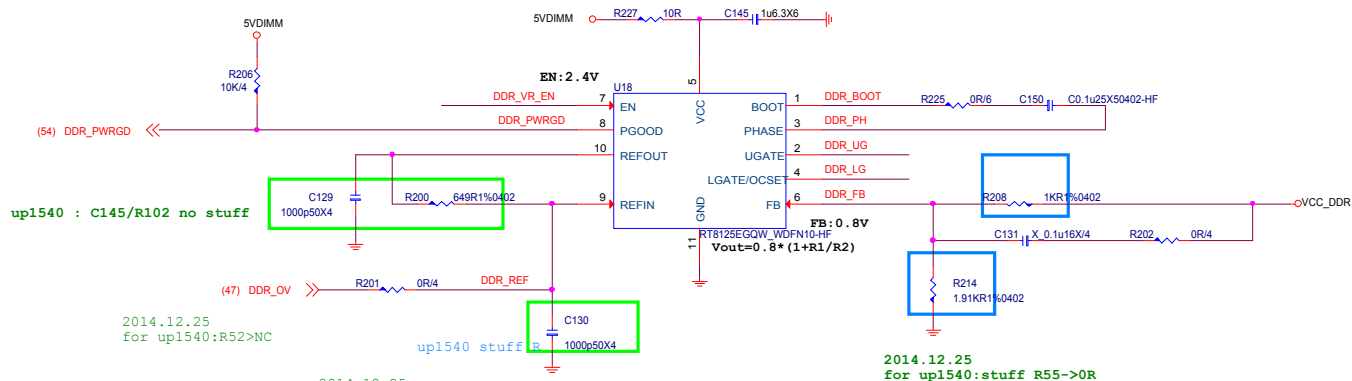
Rdson (low) 10V
D03-4C05N03-O05 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm

```

Vsa = 1.05V
ICCMAX = 11.1A
Irms = 3.14A



3.3A FOR CPU
9.5A FOR 4DIMM
1.2A FOR DDR VTT

$$\begin{aligned} \text{Rocpset} &= 4.32\text{K} \\ \text{OCP} &= \text{Rocpset} * \text{Rdson}(\text{Low side}) / 10\mu\text{A} \\ &= 8.2\text{K} * 10\mu\text{A} / 4\text{mohm} \\ &= 20.5\text{A} \end{aligned}$$


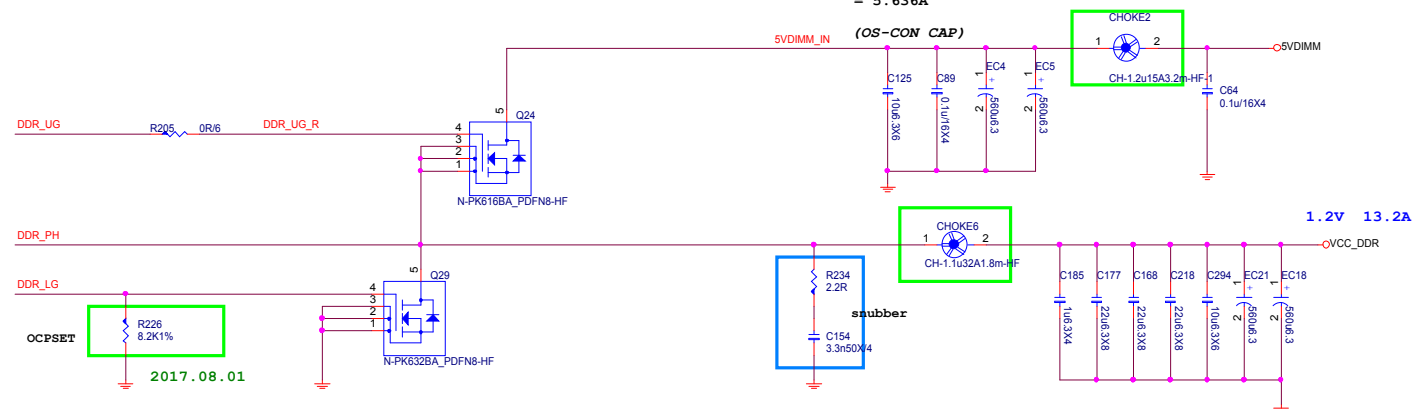
Rdson (low) 4.5V

D03-4C05N03-O05	:	5 mohm
D03-632BA0C-N03	:	4.6mohm
D03-3056M00-U47	:	6.2mohm

```
2014.12.25
for up1540:R52>NC
```

up1540 stuff R 1000p50X4

C125 is OCP set min:5K ohm
5.1K OCP SET:22.173A

$$\begin{aligned} I_{rms} &= I_{out} * \sqrt{(V_{out}/V_{in}) * [1 - (V_{out}/V_{in})]} \\ &= 13.2 * 0.427 \\ &= 5.636A \end{aligned}$$


Datasheet公式計算

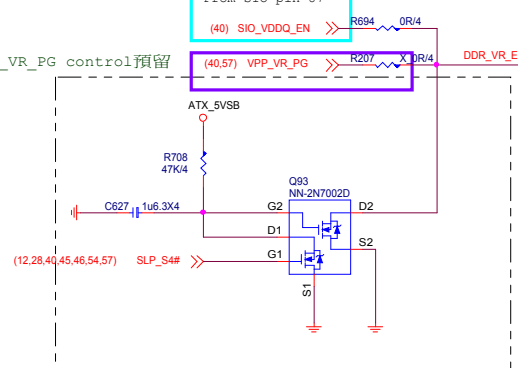
$$\begin{aligned} L_{\min} &= ((V_{\text{in}} - 1.2V) / (F_{\text{sw}} * k * I_{\text{out_max}})) * (V_{\text{out}} / V_{\text{in}}) \\ &= 0.7677\mu\text{H} \quad (K = 30\%) \end{aligned}$$

若帶入CAP ESR計算, $0.2432\mu\text{H} < L < 1.2897\mu\text{H}$

2014.12.17 update

From SIO pin 87

VPP_VR_PG_control預留



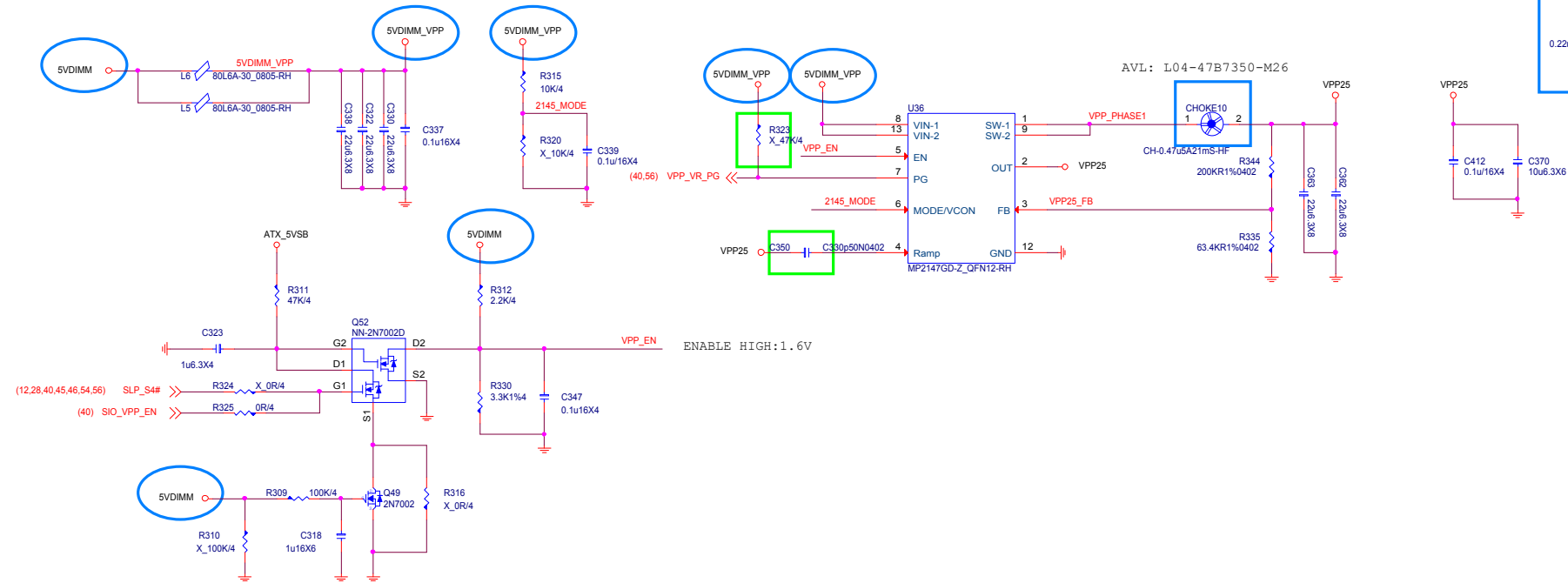
MICRO-STAR INT'L CO.,LTD

MS-7B49

Size Custom	Document Description DDR4 Power-RT8125C	Rev 1.1
Date: Tuesday, August 08, 2017		Sheet 56 of 69

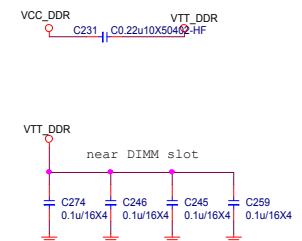
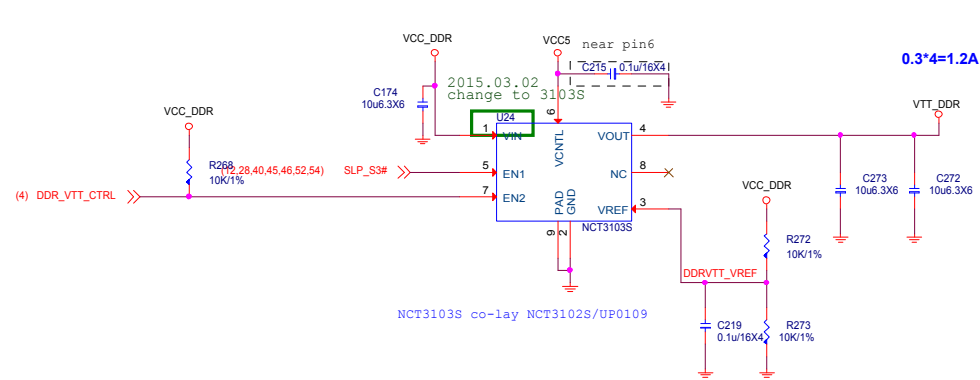
4DIMM :2.24A FOR DDR VPP2.5V

VPP25 Power
2.5V; 2.24A



To make sure VPP EN after 5VDIMM stable

DDR VTT Power



MICRO-STAR INT'L CO.,LTD

MS-7B49

Size Custom	Document Description DDR4 Power-VPP25	Rev 1.1
Date: Tuesday, August 08, 2017	Sheet 57 of 69	

PCH 1VSB

1.0V; 11A

Rocpset: 6.8K
 OCP=Rocpset*10uA/Rdson(Low side)
 =6.8K*10uA/4mohm
 =17A

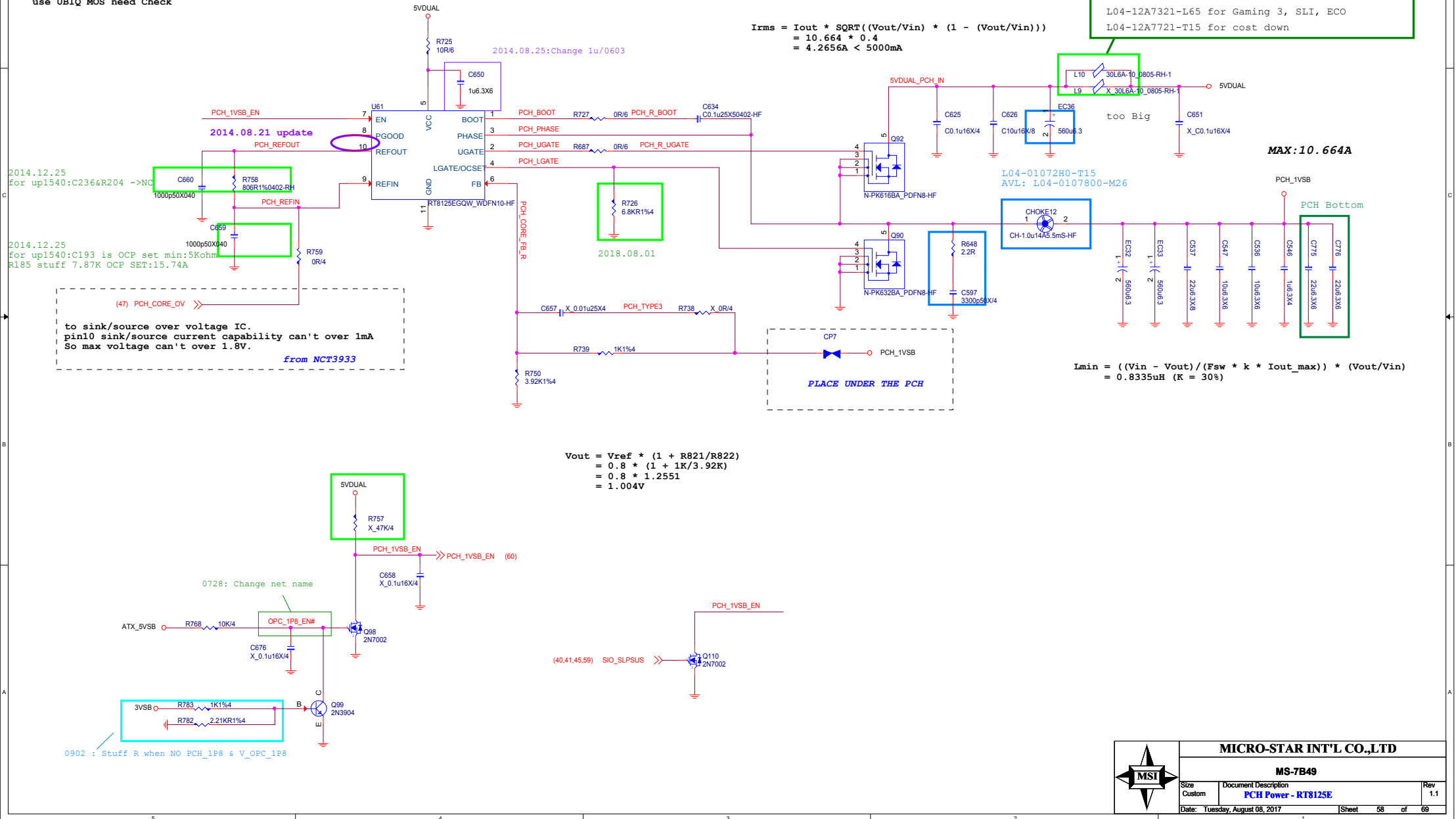
Rocs:7.87K,OCP:
D03-4C05N03-O05 : 15.74A
D03-632BA0C-N03 : 17.1A
use UBIQ MOS need Check

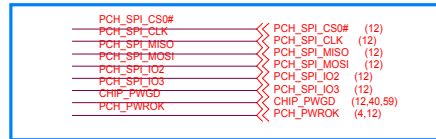
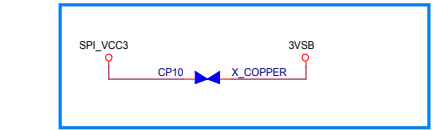
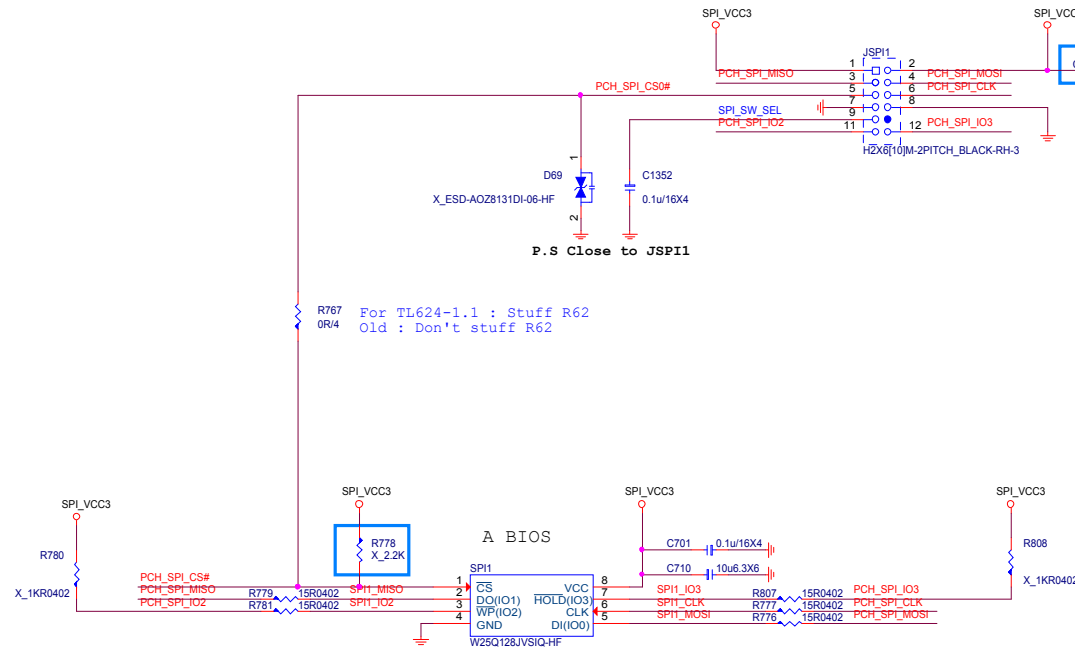
Rdson (low) 4.5V

D03-3116M00-U47 : 3.6 mohm
D03-632BA0C-N03 : 4.6mohm
D03-3056M00-U47 : 6.2mohm

$$\begin{aligned} I_{rms} &= I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))} \\ &= 10.664 * 0.4 \\ &= 4.2656A < 5000mA \end{aligned}$$

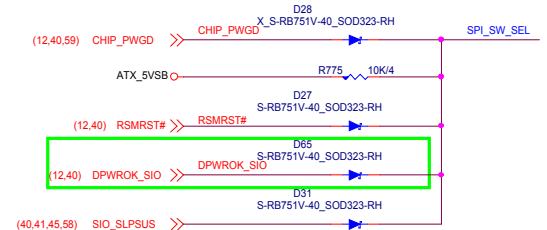
L04-47B7730-T15 for OC, Gaming 10, 9, 7, 5
L04-12A7321-L65 for Gaming 3, SLI, ECO
L04-12A7721-T15 for cost down





Module Stuff CHIP_PWGD,
But PCH_PWROK may ramp up before CHIP_PWGD.

For TL624 1.1



For TL624-1.1
SKYLAKE : Stuff D10/D17/R353
B85/H87 : Stuff D8/D9/R353
Others : Stuff R272



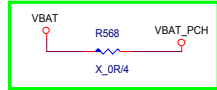
MICRO-STAR INT'L CO.,LTD

MS-7B49

Size	Document Description	Rev
Custom	SPI ROM	1.1
Date: Tuesday, August 08, 2017	Sheet 59 of 69	

20160505

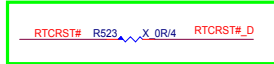
Co-Lay NOT U18 , Stuff R260



Function 1		
IN		OUT
INPUT1	INPUT2	OUTPUT1
0	1	1
1	0	0
1	1	0
0	0	0

Default

Co-Lay NOT USE U1 , R20 STUFF

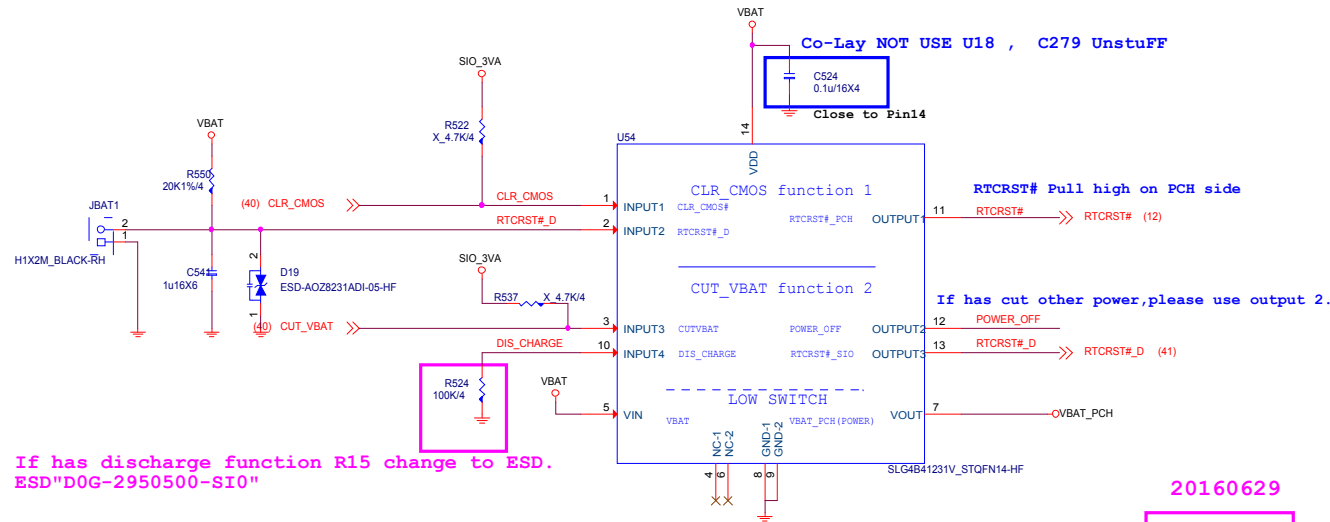


Function 2				
IN		OUT		
INPUT3 & lowswitch EN	INPUT4	OUTPUT2	OUTPUT3	VOUT
0	0	0	1	1
1	0	1	1	0 (discharge)
0	1	1	0	0 (discharge)
1	1	1	0	0 (discharge)

Default

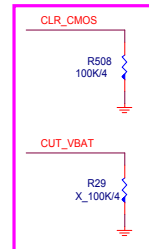
If STUFF R20 Please Check RTCRST# Double Pull High

Co-Lay NOT USE U18 , C279 Unstuff

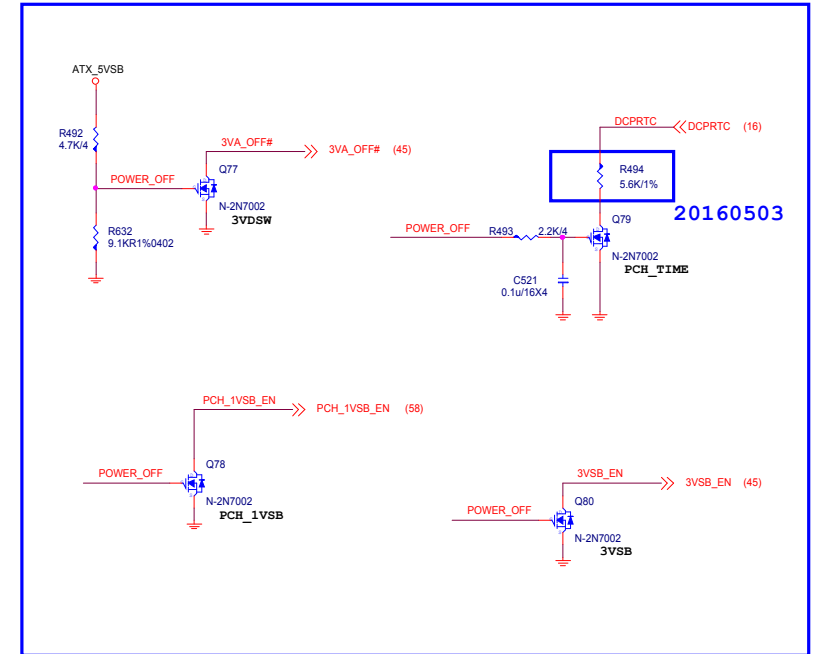


If has discharge function R15 change to ESD. ESD"D0G-2950500-SI0"

20160629



Co-Lay NOT USE U1 , ALL UNSTUFF



20160503

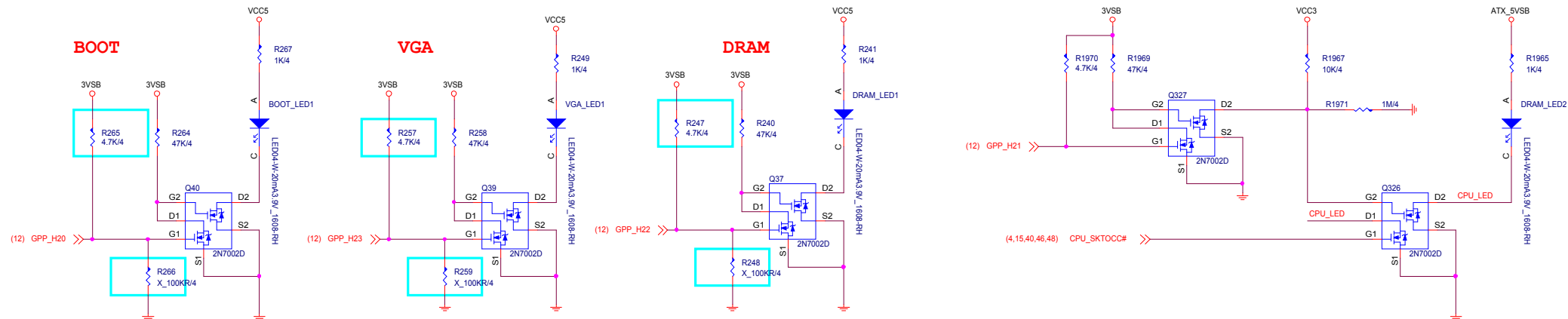


MICRO-STAR INT'L CO.,LTD

MS-7B49

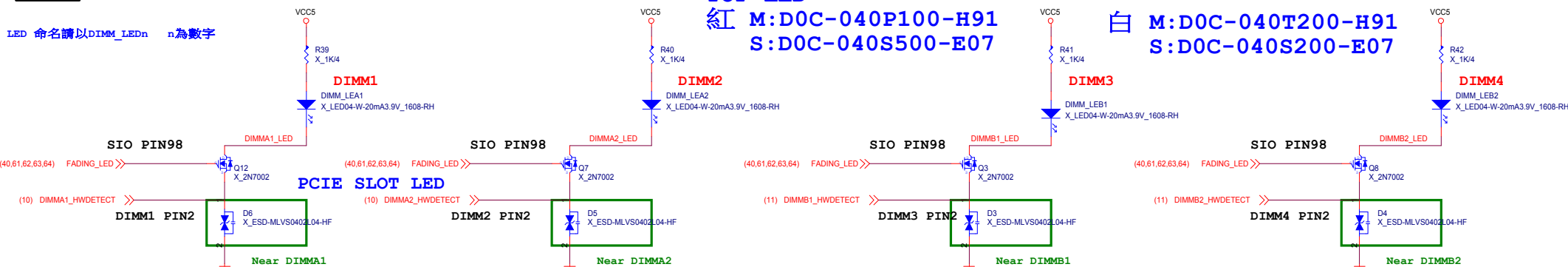
Size	Document Description	Rev
Custom	SLG46117V	1.1
Date:	Tuesday, August 08, 2017	Sheet 60 of 69

EZ Debug



DIMM

LED 命名請以DIMM_LEDn n為數字



TOP LED

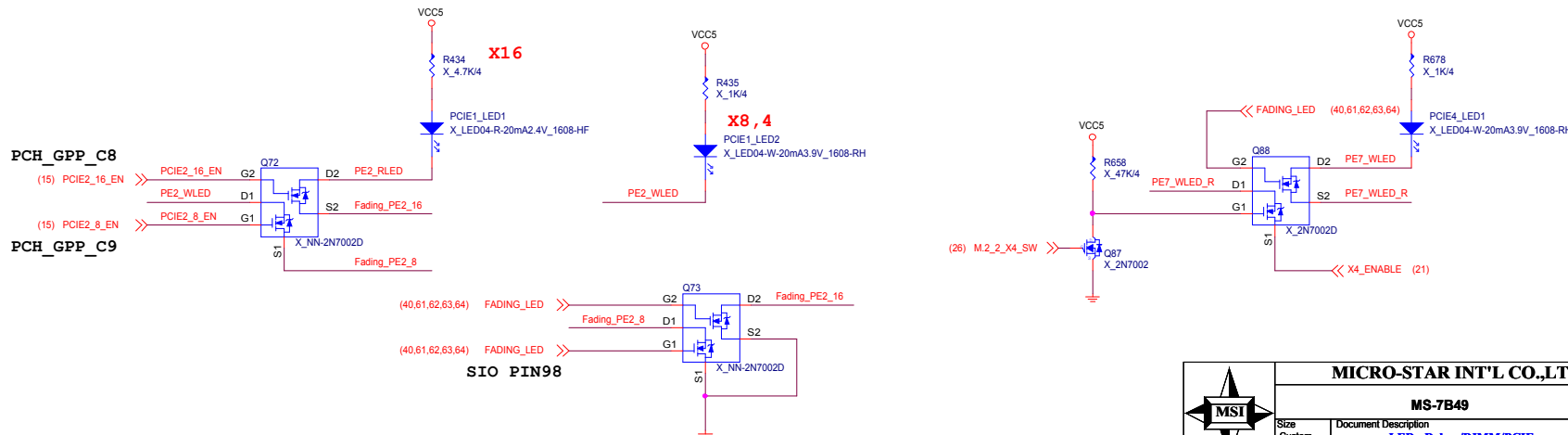
紅 M:D0C-040P100-H91
S:D0C-040S500-E07

白 M:D0C-040T200-H91
S:D0C-040S200-E07

PCIE

PCIE SLOT LED 命名請以PCIE_LEDn n為數字

GPIO LED	GPP_C8	GPP_C9
	亮 GPO PO HIGH	亮 GPO PO HIGH
滅	GPI (default LOW)	GPI (default LOW)

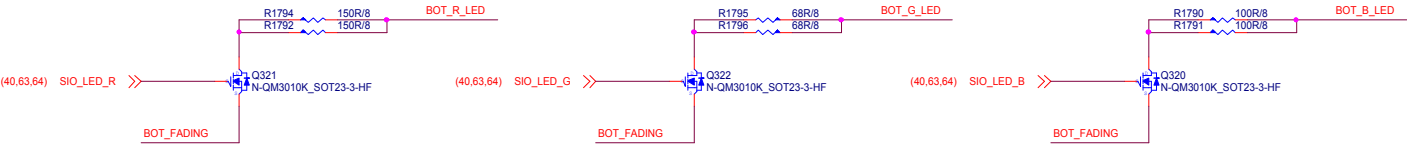
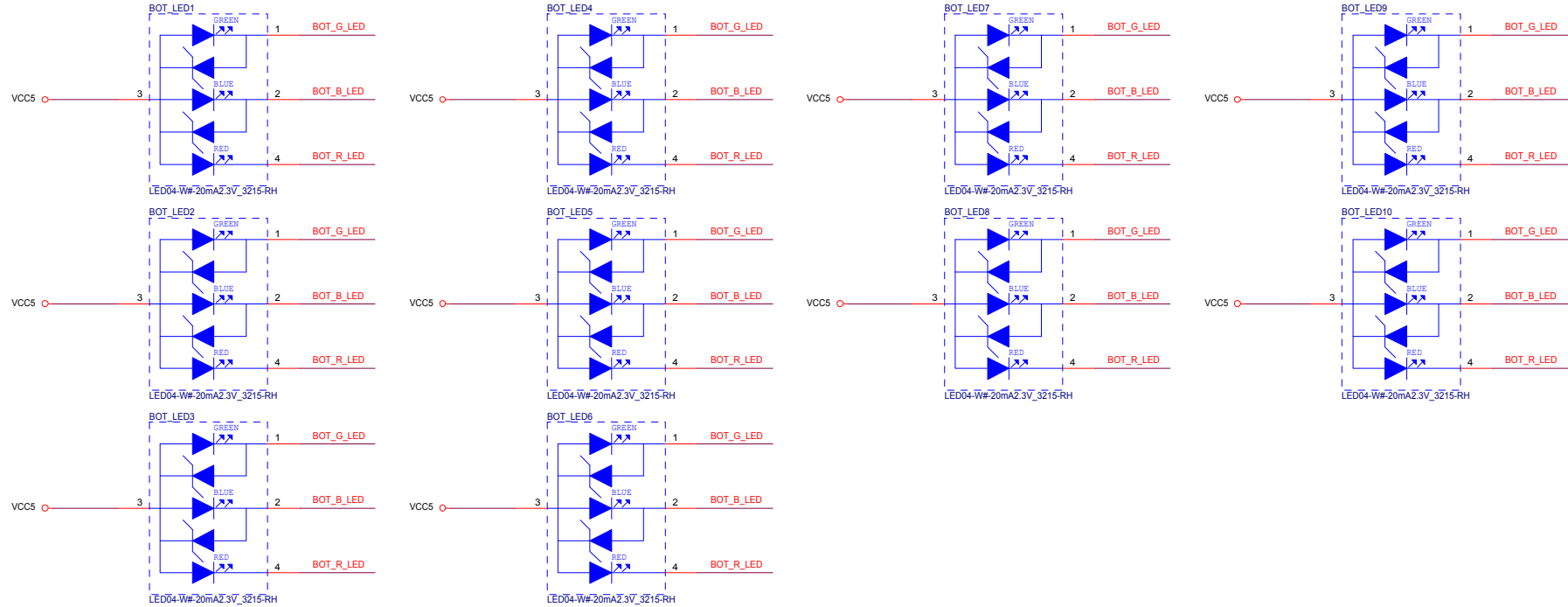


MICRO-STAR INT'L CO.,LTD

MS-7B49

Size	Document Description	Rev
Custom	LED - Debug/DIMM/PCIE	1.1
Date: Tuesday, August 08, 2017	Sheet 61 of 69	

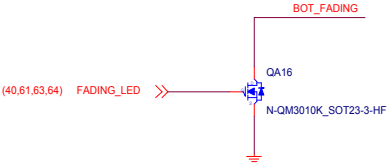
BOTTOM LED



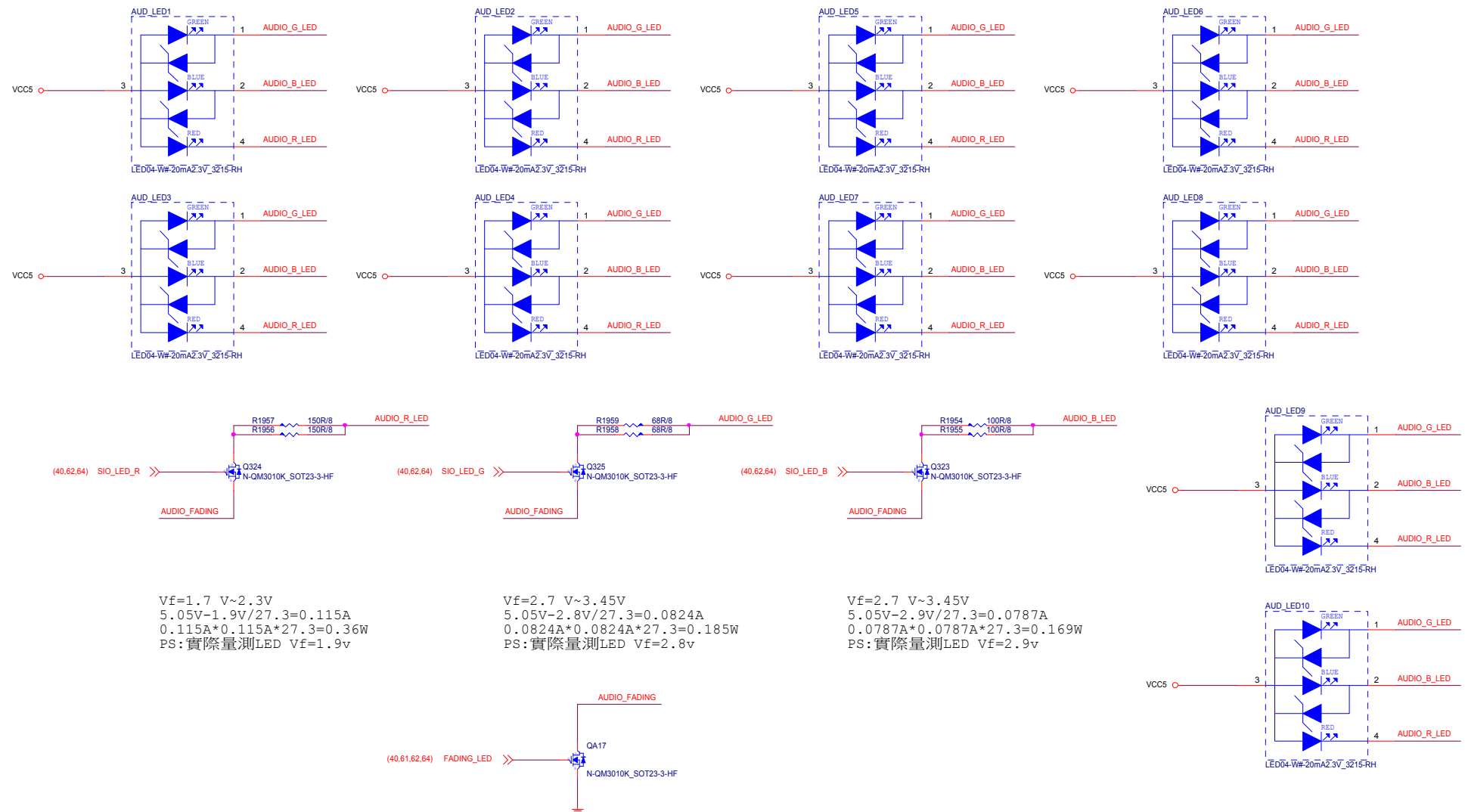
Vf=1.7 V~2.3V
5.05V-1.9V/27.3=0.115A
0.115A*0.115A*27.3=0.36W
PS:實際量測LED Vf=1.9v

Vf=2.7 V~3.45V
5.05V-2.8V/27.3=0.0824A
0.0824A*0.0824A*27.3=0.185W
PS:實際量測LED Vf=2.8v

Vf=2.7 V~3.45V
5.05V-2.9V/27.3=0.0787A
0.0787A*0.0787A*27.3=0.169W
PS:實際量測LED Vf=2.9v



AUDIO LED

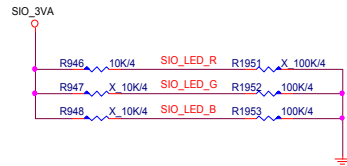
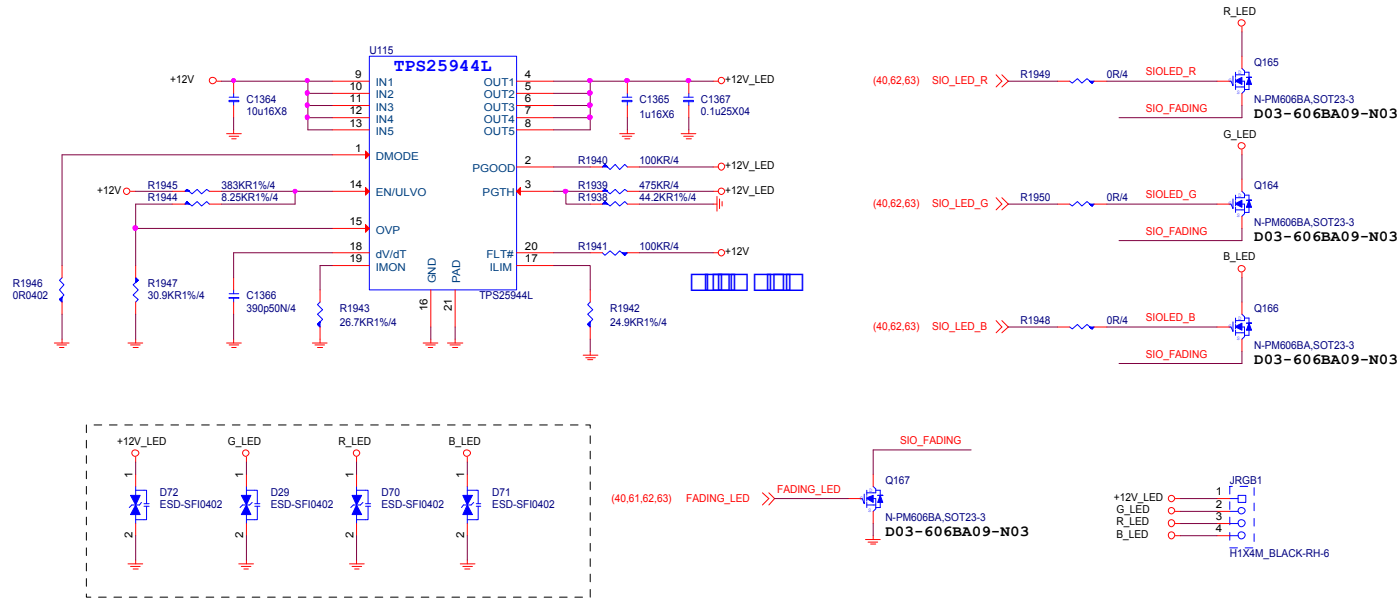


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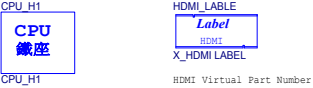
Size Custom	Document Description LED - Debug/DIMM/PCIE	Rev 1.1
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LED Control by SIO



Color	SIO_LED_R	SIO_LED_G	SIO_LED_B
RED	1	0	0
GREEN	0	1	0
BLUE	0	0	1
WHITE	1	1	1

CPU Socket



Battery



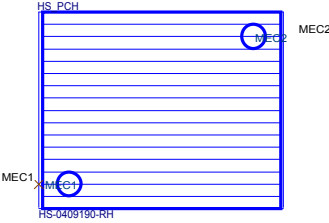
BIOS Label



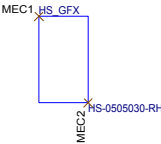
PCB



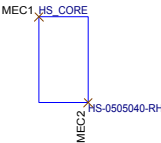
PD0-07B4911-G37, 精成-深圳, 1, 台北微星廠 (MSI)
PD0-07B4911-E48, 競華, 1, 台北微星廠 (MSI)



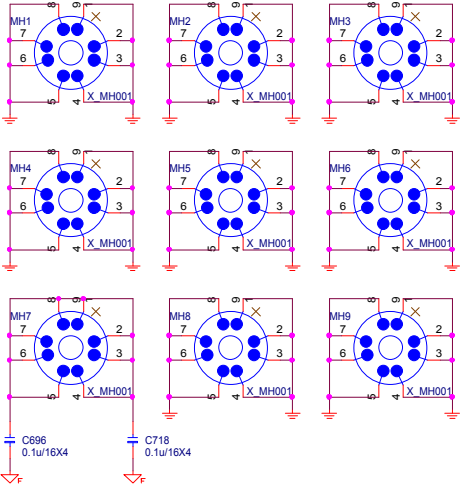
GFX Heatsink



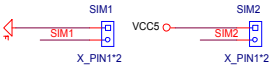
CORE Heatsink



Mounting Holes



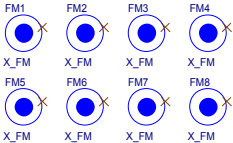
Simulation



Test point



Optical Fiducial Marks-120



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Size	Document Description	Rev
Custom	Manual parts	1.1
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To POWER 2015/02/03